SPECIFICATION

DVBT Tunter with Analog Demodulator Revision:1.1

1.SCOPE

The SDAVP-90138PE is intended for the reception of DVB-T compliant MPEG2 signals (full TES 300 744 compliant)
in combination with the tuner ,all functions are integrated to deliver a corrected stream given DVB-T encoded signal(2k 0r 8k mode)with 7MHz or 8MHz bandwidth.
Analog Demodulator (PAL B/G D/K,SECAM L,L)
Internal RF AGC for Optimal Analog performance

2.GENERAL SPECIFICATIONS

2-1. RECEIVING FREQUENCY RANGE :48.25~863.25MHz
(I^2C PLL CONTROLLER FROM OUTSIDE)

2-2. Temperature Range
Storage Temperature : -20°C ~ + 80°C
Operation Temperature : 0°C ~ + 50°C

2-3. Weight : 42g

2-4 Holding strength of ant jack
Initial Inserting Force :Max. 5.0 kg
Extracting Force After 5 Cycles :Min. 0.7 kg

3.TEST CONDITIONS

3-1. Test conditions : All data held under following conditions
: +25+/-2°C / Humidity : 45 ~ 65% RH

3-2. SUPPLY VOLTAGE :B1 5V +/-2% Ripple < 7mV
B2 1.8V +/-2% Ripple < 7mV
B3 3.3V +/-2% Ripple < 7mV
B4 5V +/-2%Ripple < 7mV

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4.Electrical Specification

NO	ITEM	CONDITION	MIN	TYP	MAX	NOTES
4.1	GENERAL SPECIFICATIONS					
4.2	Receiving frequency range (analog)		48.25		863.25	MHz
4.3	Receiving frequency range (digital)	UHF VHF HIGH	428.1 145.1		862 428	MHz
4.4	RF input impedance	IEC CONNECTOR 75 OHM				
4.5	L.O PLL synthesizer IC	MT2131 Address 0xC0				
4.6	PLL synthesizer crystal	+/- 50 ppm		16		MHz
4.7	1st intermediate frequency		1210	1220	1230	MHz
4-8	1st intermediate frequency 3dB BW	PIF (33.9MHz France A~C CH)	33.9 or 38.9 4.5			MHz MHz
4-9	1st intermediate frequency 3dB BW	9886 7.0 OP2=1 7.0 OP2=0	32.4 40.4 1.5			MHz MHz MHz
4.10	1st intermediate frequency 3dB BW	DVB-T		36.125 8		MHz MHz
4.11	Input return loss	Referred to 75 OHM 55MHz~858.25MHz LAN Gain = 0x03		6		dB
4.12	RF Max Gain			42		dB
4.13	RF Front end gain range			55		dB
4.14	phase noise	1kHz		-78		dBc/Hz
		10kHz		-84		dBc/Hz
		100kHz		-104		dBc/Hz
		1MHz		-122		dBc/Hz
4.15	Image rejection	Desired and undesired carriers of equal amplitude; undesired 88 MHz higher in frequency.		-70		dBc
4.16	CSO	Input 133 CW carriers @ +15dBmV,IF gain control voltage at for 1VP-P output		-59		dBc
4.17	CTB			-62		dBc
4.18	Spurious			-59		dBc
4.19	Cross modulation	132 undesired carriers 100% AM modulated at 15.75kHz		-56		dBc
4.20	Output carrier-to-noise ratio (VGA Out)	Measured in a 6 MHz bandwidth		-50		dB
4.21	Output carrier-to-noise ratio (Down-Converter Out)	Measured in a 4.2 MHz bandwidth		-53.6		dB
4.22	Noise Figure,CATV mode	Maximum gain		7		dB
4.23	Noise Figure,Off-Air mode	Maximum gain		6		dB
4.24	Adjacent channel rejection,N	Undesired NTSC into desired ATSC, -68dBm ATSC channel input level		-45		dBc
		Undesired ATSC into desired ATSC, -68dBm ATSC channel input level		-39		dBc
4.25	Adjacent channel rejection,N	Undesired NTSC into desired ATSC, -68dBm ATSC channel input level		-58		dBc
		Undesired ATSC into desired ATSC, -68dBm ATSC channel input level		-57		dBc
4.26	CONSUMPTION CURRENT	: B1 5V B2 1.8V B3 3.3V B4 5V		260 170 120 81		mA mA mA mA

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NO	ITEM		CONDITION	MIN.	TYP.	MAX.	NOTES
5.1	Analog Electrical Characterisitics Control refer to TDA9886 data sheet						
5.1.1	SENSITIVITY		S/N=30dB 100% White pattern, PAL:87.5% S/N=30dB 100% White pattern, SECAM:90%		47 51	45 43	dBuV dBuV
5.1.2	VIDEO OUT LEVEL		color bar pattern, PAL:87.5% color bar pattern, SECAM:90%	1.5 1.4	1.8 1.7	2.1 2.0	Vp-p Vp-p
5.1.3	Video Frequency Response 0.8 MHz 1.8 MHz 2.8 MHz 3.0 MHz 3.8 MHz		Video Signal : 87.5% AM Mod. Multi- Burst Signal at CH.14 (471.25MHz)	 -2.0 -2.0 -3.0 -4.0 -4.0	 0 0 0 -1.0 -1.0	 +1.0 +1.5 +1.5 +1.5 +1.5	 dB dB dB dB dB
5.1.4	VIDEO S/N		INPUT LEVEL 70dBuV 100% White pattern,PAL:87.5% INPUT LEVEL 70dBuV 100% White pattern,PAL:87.5%	42 40	45 43		dB dB
5.1.5	Chroma Distortion	DP DG	5 Step Linearity Signal 87.5% mod. Ref. 471.25MHz LEVEL:70dBuV		+/-2 +/-3	+/-5 +/-5	Deg %
5.1.6	AUDIO OUTPUT LEVEL		AUDIO GAIN 0dB ADJUST MODE Bit 7 - 6dB		1.0 0.6		Vp-p
5.1.7	AUDIO S/N		INPUT LEVEL 70dBuV		42		dB
5.1.8	AUDIO THD (TOTAL HARMONIC DISTORTION)				0.5		%
5.1.9	AUDIO OUTPUT 3dB RESPONSE De-emphasis 70us		AUDIO De-emphasis ADJUST MODE BIT6,5	90	90		KHz
5.1.10	AUDIO 2nd SIF OUTPUT LEVEL			0.3	0.4		Vp-p
5.1.11	SIF OUT Level		Video mod : 0FF Video Signal : 70dBuV Sound Signal : 63dBuV	420	500	580	mVp-p
5.2	Digital Electrical characterisitics Control refer to AF9013 data sheet chip address 0x38						
5.2.1	Input sensitivity		Band width 7MHz or 8MHz FET mode 2K Guard interal 1/32 Constllation 64QAm FEC code rate 2/3 RS uncorrected error=0		-76		dBm
5.2.2	Performance with AWGN		C/N at antenna input input		20		dm
5.2.3	protection from co-channel PAL		PAL-I 75% bars,FM sound 1KHz		4		dB
5.2.4	protection from adjacent channel PAL		PAL-I 75% color bars,FM sound 1KHz		-35		dB
5.2.5	protection from adjacent DVB-t				-25		dB
5.2.6	protection from image Channel PAL		PAL-I 75% color bars,FM sound 1KHz		-46		dB
5.2.7	Pecformance with single echo inside the interval 2K mode		Te=Tg included (7.2us) Delay phase=0°		1.5		dB
5.2.8	Performance with single echo inside the interval		Te-Tsymbo 1/ 2 Delay phase=0°		19.5		dB
5.2.9	Typical multi-path channel		Additional END		4.0		dB

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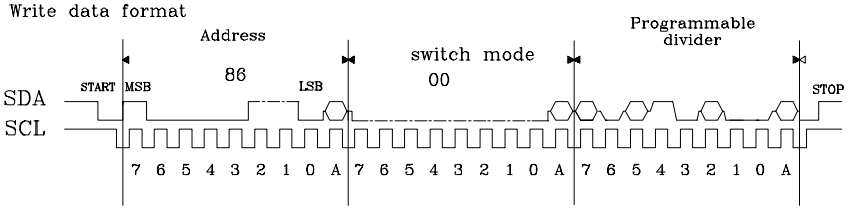
6.0 IF PROGRMMING

A detailed description of the I²C-bus specification, with application, is given in date sheet of the TDA9886

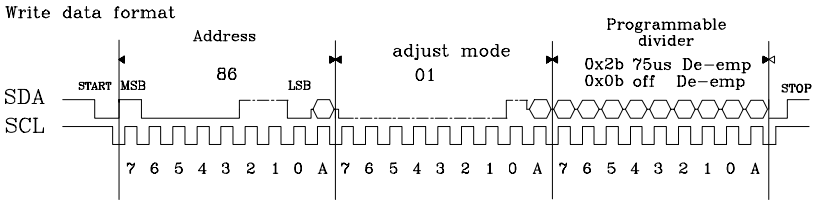
Notice: To get good video S/N for analog signal receiving, please set up digital demodulator as following power off mode .

Write data format



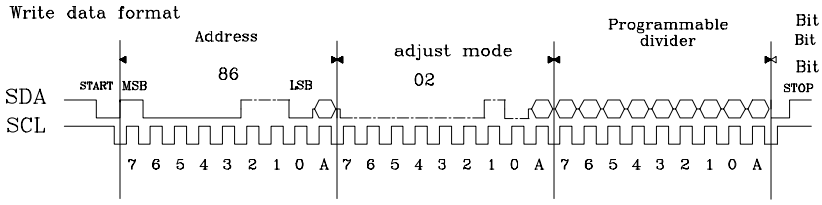
Bit 7=0 (SIF) FREQ 40.4MHz (SAW2 MODE)
FREQ 32.4MHz (SAW2 MODE)
Bit 6=0 (fix)
Bit 5=1 audio mute on
5=0 audio mute off
Bit 4=1 (fix)
Bit 3=0 (fiX)
Bit 2=1 (SIF) SAW2 MODE (PIF 33.9 or 38.9)
2=0 (SIF) SAW1 MODE (PIF 38.9 ONLY)
Bit 1=0 (fix)
Bit 0=0 (fix)

Write data format



Bit 7=1 audio gain −6dB
7=0 audio gain −0dB
Bit 6=1 50us audio De-emphasis
6=0 75us audio De-emphasis
Bit 5=1 on De-emphasis
5=0 off De-emphasis
Bit 4,3,2,1,0
1, 1 , 1 , 1 , 1 TOP ADJUSTMENT +15
|
0, 0 , 0 , 0 , 0 TOP ADJUSTMENT −16

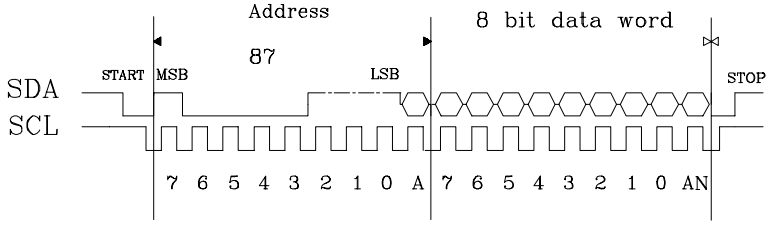
Write data format



Bit 7=0 (fix)
Bit 6=1 gating in case of 36% Positive modulation
6=0 gating in case of 0% Positive modulation
Bit 5=0 (fix)
Bit 4,3,2 0,1,0 (38.9MHz)
1,0,0 (33.9MHz France A~C ch)
Bit 1,0
0 0 = SIF 4.5MHz NTSC M
0 1 = SIF 5.5MHz PAL B/G
1 0 = SIF 6.0MHz PAL I
1 1 = SIF 6.5MHz PAL D

Bit 7 =1 VCO IN +/− 1.6MHz WINDOW AFT
7 =0 VCO OUT +/− 1.6MHz WINDOW AFT
Bit 6 =1 HIGH LEVEL VIF >200uV
6 =0 LO LEVEL VIF
Bit 5 =1 detection
5 =0 on detection

Read data format



bit 4,3,2,1		
0 1 1 1	AFC <	−187.5KHz
0 1 1 0		−162.5
0 1 0 1		−137.5
0 1 0 0		−112.5
0 0 1 1		−87.5
0 0 1 0		−62.5
0 0 0 1		−37.5
0 0 0 0		−12.5
1 1 1 1		+1.25
1 1 1 0		+37.5
1 1 0 1		+62.5
1 1 0 0		+87.5
1 0 1 1		+112.5
1 0 1 0		+137.5
1 0 0 1		+162.5
1 0 0 0	>	+187.5

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6.0 TUNER PLL PROGRAMMING

Table Serial Communications Register Map

	REGISTER ADDRESS	MSB B7	B6	B5	B4	B3	B2	B1	LSB B0	DEF
Part/ Rev	00	PART/REV								0x3F
LO1C 1	01	NUM1(12-5)								0x50
LO1C 2	02	0	0	0	NUM1(4-0)					0x00
LO1C 3	03	DIV1								0x50
LO2C 1	04	NUM2(4-0)								0x80
LO2C 2	05	0	0	0	NUM2(4-0)					0x00
LO2C 3	06	0	DIV2							0x49
PWR	07	RFAGCen	UPCen	DNCen	VGCen	FDCen	AFCen	SROen	GPO	0xF2
LO Status	08	LO1LK	LO1AD			LO2LK	LO2AD			XX
AFC Status	09	AGCdone	VGAGOK	PD1			PD2			XX
TEMP	0A	XLOW	AFCAD			TEMP				XX
UPC 1	0B	0	LNAGain		Band					0x61
UPC 2	0C	UPCIbuf		UPCImix		UPCILAN		gcATTN (1-0)		0x04
AGC 1	0D	gcATTN(9-2)								0x00
AGC 2	0E	0	gcRL							0x00
AGC 3	0F	gcDNC								0x00
AGC 4	10	AGCfrz	gcRLma							0x7F
AGC 5	11	gcDNCmax								0x00
AGC 6	12	PD1lev			0	1	0	1	0	0x8A
AGC 7	13	PD2lev			1	1	1	0	0	0x9C
Misc Cntl 1	14	0	VGAHiGain	VGAI		DNCILO		DNCIbuf		0x00
Misc Cntl 2	15	0	AGCRST	0	0	1	PD1LevEx	XDIVE		0x0C
LO Cntl	16	LO1en	0	1	0	LO2en	0	1	0	0xAA
Reserved	17	0	1	1	1	1	0	0	0	0x78
Reserved	18	1	0	0	0	0	0	0	0	0x80
Reserved	19	1	1	1	1	1	1	1	1	0xFF
Reserved	1A	0	1	1	0	1	0	0	0	0x68
Reserved	1B	1	0	1	0	0	0	0	0	0xA0
Reserved	1C	1	1	1	1	1	1	1	1	0xFF
Reserved	1D	1	1	0	1	1	1	0	1	0xDD
Reserved	1E	0	0	0	0	0	0	0	0	0x00
Test 2d	1F	Cap Trim								0x00

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6.1

FIELD	REGISTER	R/W	BITS	DEFAULT	DESCRIPTION
PART/REV	Part/Rev	R	8	0x3E	Part/Rev Code
NUM1	LO1C 1,2	R/W	13	0x0500	LO1 FracN Numerator
DIV1	LO1C 3	R/W	8	0x50	LO1 Divider $f_{LO1} = f_{SRO}$ (DIV1 + NUM1÷8191)
NUM2	LO2C 1,2	R/W	13	0x8000	LO2 FracN Numerator
DIV2	LO2C 3	R/W	7	0x49	LO2 Divider $f_{LO2} = f_{SRO}$ (DIV2 + NUM2÷8191)
RFAGC	PWR	R/W	1	0x01	Enable automatic RF AGC
UPCen	PWR	R/W	1	0x01	Enable Up-converter / LO1
DNCen	PWR	R/W	1	0x01	Enable Down-converter / FGA / LO2
VGAen	PWR	R/W	1	0x01	Enable Variable Gain Amplifier
FDCen	PWR	R/W	1	0x00	Enable Forward Data Channel Amplifier
AFCen	PWR	R/W	1	0x00	Enable AFC A/D
SROen	PWR	R/W	1	0x00	Enable SRO
GPO	PWR	R/W	1	0x00	General-purpose Input / Output
LO1LK	LO Status	R	1	-	LO1 PLL Lock Status (0=Unlocked, 1=Locked)
LO1AD	LO Status	R	3	-	LO1 VCO Voltage: 0:V_{CMTANK} 0.9 < V_{TUNE} < V_{CMTANK} 0.1 2:V_{CMTANK} 1.1 < V_{TUNE} < V_{CMTANK} 0.9 3:V_{TUNE} < V_{CMTANK} 1.1 4:V_{CMTANK} 0.1< V_{TUNE} <V_{CMTANK} 5:V_{TUNE}>V_{CMTANK}
LO2LK	LO Status	R	1	-	LO2 PLL Lock Status (0=Unlocked, 1=Locked)
LO2AD	LO Status	R	3	-	LO2 VCO Voltage: 0:V_{CMTANK} 0.9 < V_{TUNE} < V_{CMTANK} 0.1 2:V_{CMTANK} 1.1 < V_{TUNE} < V_{CMTANK} 0.9 3:V_{TUNE} < V_{CMTANK} 1.1 4:V_{CMTANK} 0.1< V_{TUNE} <V_{CMTANK} 5:V_{TUNE}>V_{CMTANK}
AGCdone	AFC Status	R	1	-	AGC Settled
VGAGOK	AFC Status	R	1	-	VGA gain status: 0:VGAHiGain wants to be in opposite state 1:VGAHiGain current state is OK
PD1	AFC Status	R	3	-	PD1 A/D Converter Output
PD2	AFC Status	R	3	-	PD2 A/D Converter Output
XLOW	TEMP Status	R	1	-	SRO Amplitude Status (0 = Low, 1 = OK)
AFCAD	TEMP Status	R	3	-	AFC A/D Output: 0 : < 0.75 Vdc 1 : 0.75 Vdc - 1.50 Vdc 2 : 1.50 Vdc - 2.25 Vdc 3 : 2.25 Vdc 3.00 Vdc 4 : > 3.00 Vdc
TEMP	TEMP Status	R	4	-	Temperature Readout: T = 35 + (5 x N) °C

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6.2.1

FIELD	REGISTER	R/W	BITS	DEFAULT	DESCRIPTION
LNAGain	UPC 1	R/W	2	0x03	LNA Gain Block 0 : 0.0dB 1 : -1.6dB 2 : -2.7dB 3 : -3.7dB
Band	UPC 1	R/W	2	0x00	Input Filter Band Center Frequency(nomical, centers moved by Cap Teim result): 0 : 55 MHz 1 : 110 MHz 2 : 165 MHz 3 : 220 MHz 4 : 275 MHz 5 : 330 MHz 6 : 385 MHz 7 : 440 MHz 8 : 495 MHz 9 : 550 MHz 10 : 605 MHz 11 : 660 MHz 12 : 715 MHz 13 : 770 MHz 14 : 825 MHz 15 : 880 MHz 16 : 935 MHz 17 : 990 MHz 18 : 1045 MHz 19 : 1100 MHz
UPCIbuf	UPC 2	R/W	2	0x00	Upconverter LO Buffer Current
UPCImix	UPC 2	R/W	2	0x00	Upconverter LO Output Amplifier Current
UPCILNA	UPC 2	R/W	2	0x00	Upconverter LNA Current: 0 : 21.9 mA 1 : 16.0 mA 2 : 9.4 mA 3 : 3.1 mA
gcATTN	AGC 1,UPC 2	R/W	10	0x000	Front-End Attenuator Digital Gain Control (valid range 0 0X2FF)
gcRL	AGC 2	R/W	7	0x00	LNA Rloads Digital Gain Control
gcDNC	AGC 3	R/W	8	0x00	Downconverter Digital Cain Control
AGCfrz	AGC 4	R/W	1	0x00	Freeze AGC at its Current State
gcRLmax	AGC 4	R/W	7	0x7F	Maximum gcRL value before switching to gcATTN
gcDNCmax	AGC 5	R/W	8	0x00	Maximum gcDNC value before switching to gcRL
PD1lev	AGC 6	R/W	3	0x04	PD1 desired input level:
PD2lev	AGC 7	R/W	3	0x04	PD2 desired input level:
VGAHiGain	Misc Cntl 1	R/W	1	0x00	VGA High-Gain Mode
VGAI	Misc Cntl 1	R/W	1	0x00	VGA Bias Current:
DNCILO	Misc Cntl 1	R/W	2	0x00	Downconverter LO Buffer Current: 0 : 750 uA 1 : 600 uA 2 : 450 uA 3 : 250 uA

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6.2.2

FIELD	REGISTER	R/W	BITS	DEFAULT	DESCRIPTION
DNCIbuf	Misc Cntl 1	R/W	2	0x00	Downconverter Output Buffer Current : 0 : 940 uA 1 : 753 uA 2 : 565 uA 3 : 315 uA
LOrst	Misc Cntl 2	R/W	1	0x00	Reset VCO and Fractional-N accumulators
AGCrst	Misc Cntl 2	R/W	1	0x00	Reset RF AGC
CAPTrst	Misc Cntl 2	R/W	1	0x00	Start a Cap Trim Cycle
AUTOVGAg	Misc Cntl 2	R/W	1	0x01	Automatic VGA gain
PD1LevEx	Misc Cntl 2	R/W	1	0x00	Shift PD1 level upward
XDIVE	Misc Cntl 2	R/W	2	0x00	SRO external divider (0=OFF, 1= ÷4,2= ÷2,3= ÷1)
LO1en	LO Cntl	R/W	1	0x01	Enable LO1 VCO (0=disable, 1=enable)
LO2en	LO Cntl	R/W	1	0x01	Enable LO2 VCO (0=disable, 1=enable)
Cap Trim	Test 2	R/W	8	0x00	Results of Cap Trim cycle

7. **Electorstic discharge**

7.1 **Test**

Each front-end must be capable of normal performance following its subjection to the following tests:

MIL STD 883C HBM

Test is performed with a voltage discharge from a 100 **PF** capacitor over a 1500 **OHM** series resistance in the discharge path. There is a direct contact between the test probe head and the unit under test, using the test points and conditions detailed below:

o Test to pins 1 through 22:
3 successive ESD discharges of **+/-2 KVDC** between each pin and the front-end frame.

IEC 1000-4-2

Test is performed with a voltage discharge from a 150 **PF** capacitor over a 330 **OHM** series resistance in the discharge path. There is a direct contact between the test probe head and the unit under test, using the test points and conditions detailed below:

o Test for antenna input socket +/-8 **KVDC**

7.2 **Handling**

Anyone handling a front-end must wear a properly grounded anti-static discharge bracelet to minimize **ESD** damage.
After each front-end is aligned and tested, it will be packed with anti-static material prior to transportation and storage. This package is to remain in place until the front-end is assembled and soldered onto the receiver main board.

8 **Reliability test procedure & conditions**

Note:Room temperature = 25°C +/- 2°C

8.1 **Heat load test**

- o Measure the DUTs at room temperature
- o Load the DUTs into chamber of the following conditions:

Temperature	=	60 °C
Period	=	500 hrs
Cycle	=	1.5 hrs on; 0.5 hrs off
Quantity	=	10 pcs

- o Cool-down 0.5 hr at room temperature, then measured the DUTs within 1 hr
- o The test shall be continued to 1000 cycles for information only

8.2 **Humidity load test**

- o Measure the DUTs at room temperature
- o Load the DUTs into chamber of the following conditions:

Temperature	=	40 +/- 5 °C
Period	=	24 hrs
Cycle	=	constantly on
Quantity	=	24 pcs

- o Cool-down 0.5 hr at room temperature, then measured the DUTs within 1 hr
- o Load the DUTs again into chamber of the following conditions:

Temperature	=	40+/-5°C
Humidity	=	90 to 95%
Period	=	500 hrs
Cycle	=	1.5 hrs on; 0.5 hr off
Quantity	=	20 pcs

- o Cool down 0.5hr at room temperature, then measured the DUTs within 1 hr

8.3 **Cold test**

- o Measure the DUTs at room temperature
- o Load the DUTs into chamber of the following conditions:

Temperature = -2 +/-5 °C
Period = 500 hrs
Cycle = constantly on
Quantity = 10 pcs

- o Warm up for 2 hrs at room temperature, then measured the DUTs within 1 hr

8.4 **Thermal shock**

- o Measure the DUTs at room temperature
- o Load the DUTs into chamber of the following conditions:

Temperature = -25°C for 60 min
↓ ↑
80°C for 60 min
Period = 200 cycles
Power = power off
Quantity = 10 pcs

- o Cool-down 0,5 hr at room temperature then measured the DUTs within 1 hr

8.5 **Temperature cycle test**

- o Measure the DUTs at room temperature
- o Load the DUTs into chamber of the following conditions:

Temperature = -5°C for 16 hrs then 60°C for 8 hrs
Period = 500 hrs
Cycle = constantly on
Quantity = 10pcs

- o Cool down 0.5 hr at room temperature, then measured the DUTs within 1 hr
- o Load the DUTs again into chamber of the following conditions:

Temperature = 40 +/- 5°C
Humidity = 90 to 95%
Period = 500 hrs
Cycle = 1.5 hrs on; 0.5 hrs off
Quantity = 10 pcs

- o Cool down 0.5 hr at room temperature, then measured the DUTs within 1hr

8.6 **Vibration test**

- o Frequency: 3.5 Hz
- o Vertical amplitude: 15 to 25 mm
- o Duration: 1 hr
- o Quantity: 1 carton

8.7 **Drop test**

- o Packaged apparatus: <or = 50 kg
- o Height: depend on weight
- o 1 corner + 3 edge + 6 faces

Drop on the weakest corner (point G)
Drop on the shortest edge on contact with point G
Drop on average edge in contact with point G
Drop on the longest edge in contact with point G
Drop flat wise on the side of minimum surface
Drop flat wise on the side of opposite minimum surface
Drop flat wise on the side of average surface
Drop flat wise on the side of opposite average surface
Drop flat wise on the side of maximum surface
Drop flat wise on the side of opposite maximum surface

- o Quantity :1 carton

8.8 Life test

- o Measure the DUTs at room temperature
- o Load the DUTs into chamber of the following conditions:

Temperature = 60 °C
Period = 500 hrs
Cycle = constantly on
Quantity = 20 pcs

- o Cool down 0.5 hr at room temperature, then measure the DUTs within 1hr

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9.0 Application

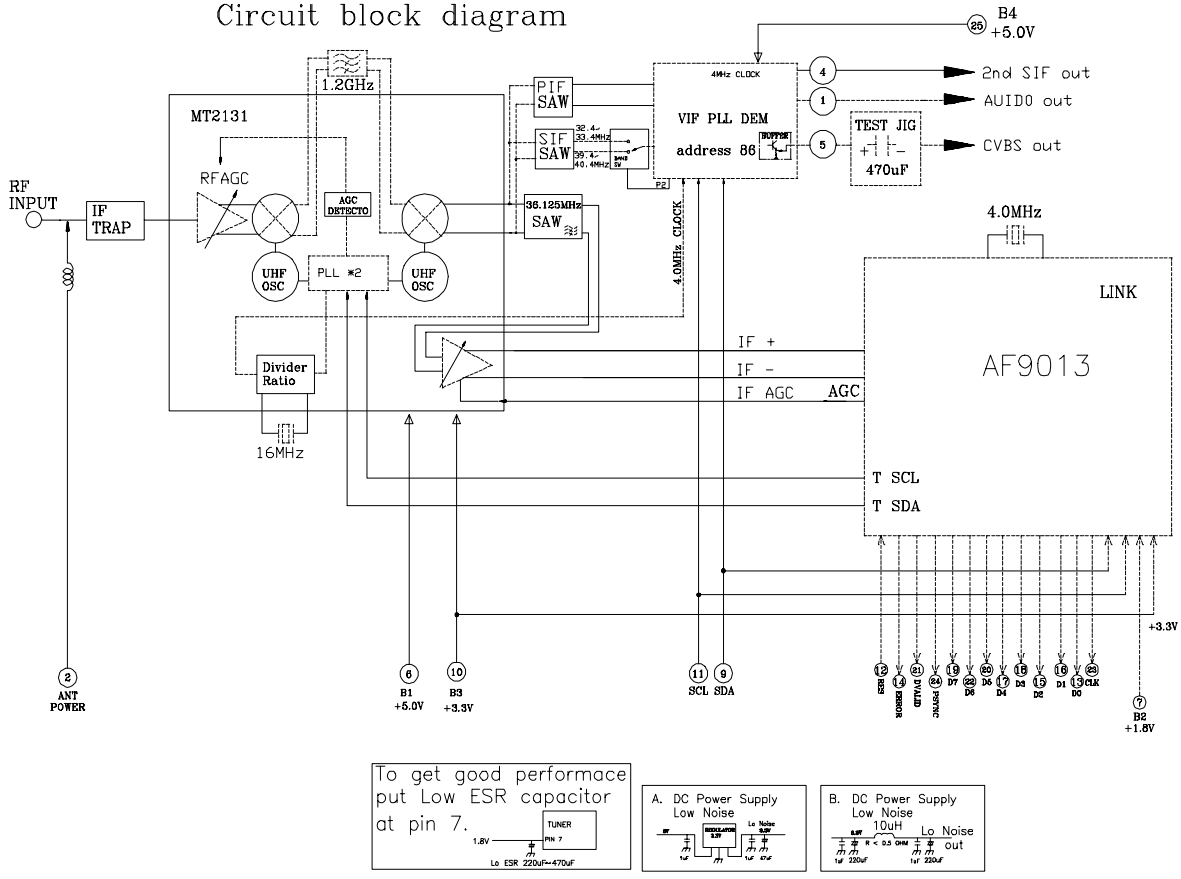
Pin 25 (B4 + 5.0 V) is power supply for analog demodulator TDA9886.

Pin 25 can be switched off when it is under digital mode.

Pin 7 (B2 + 1.8 V) is power supply for DVB-T demodulator AF9013.

Pin 7 can be switched off when it is under analog mode.

Circuit block diagram



SPECIFICATION

DVBT Tunter with Analog Demodulator Revision:1.1

PIN NO.	CONTENTS
1	AUDIO
2	ANT POWER
3	GND
4	SIF
5	CVBS
6	B1 +5.0V
7	B2 +1.8V
8	GND
9	SDA
10	B3 +3.3V
11	SCL
12	RESET
13	D0

PIN NO.	CONTENTS
14	ERROR
15	D2
16	D1
17	D4
18	D3
19	D7
20	D5
21	DVALID
22	D6
23	CLK
24	PSYNC
25	B4 +5.0V
26	GND

CUSTOM MODEL	
COMTECH MODEL	SDAVP-90138PE