SPECIFICATION

DMB TH Revision:1.0

1.SCOPE

The PDMB-TH8G is intended for the reception of TDS-OFDM (Time Domain Synchonous Orthogonal Frequency Division Multiplexing) demodulator. The demodulator is fully compliant with DMB-TH (Digital Multimedia Broadcasting Terrestrial/Handheld)
The main parameters may be detected and configured automatically or manually.
The main configurable parameter for GB20600-2006 are:

* Sub-carrier demodulation: 4QAM-NR, 4QAM, 16QAM, 32QAM, or 64QAM
* Forward error correction rate: 0.4, 0.6, or 0.8
* Guard interval: PN420,PN595, and PN945
* Time De-interleaving: M=240 or M=720.
* Channel bandwidth: 8MHz

2.GENERAL SPECIFICATIONS

2-1. RECEIVING FREQUENCY RANGE UHF474~858MHz
(I^2C PLL CONTROLLER FROM outside)

2-2. Temperature Range

Storage Temperature	:	-20°C ~ + 80°C
Operation Temperature	:	0°C ~ + 60°C

2-3. Weight : 10.3g

3.TEST CONDITIONS

3-1. Test conditions : All data held under following conditions
: +25+/-2°C / Humidity : 45 ~ 65% RH

3-2. SUPPLY VOLTAGE

B1	2.8V	+/-2% Ripple < 7mV
:B2	1.2V	+/-2% Ripple < 7mV
B3	2.8V	+/-2% Ripple < 7mV

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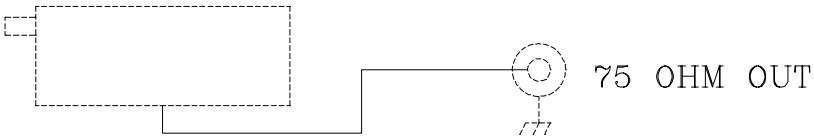
4.Electrical Specification

NO	ITEM	CONDITION	MIN	TYP	MAX	NOTES
4-1.	GENERAL SPECIFICATIONS					
4-2.	Receiving frequency range	UHF SEE table 8-12	474		858	MHz
4-3.	Mergin frequency	UHF	-6		+3	MHz
4-4.	RF input impedance	IPEX CONNECTOR 75 OHM				
4-5	L.O PLL synthesizer IC	TUA6039 Address 0xC0				
4-6	PLL synthesizer crystal	+/- 30 ppm		4.0		MHz
4.7	1st intermediate frequency 3dB BW	DMBT		36 8		MHz MHz
4-8	AGC voltage input external	0V to 5V 0V min gain 5V max gain				Current 20uA max
4-9	CONSUMPTION CURRENT	B1 2.8V B2 1.2V B3 2.8V		97 198 142		mA mA mA
4-10	IF Test circuit					
4-11	Noise Figure	UHF		7	9	dB
4-12	AGC Range AGC voltage 5V to 0.5V	UHF	35	55		dB dB
4-13	Gain taper				8	dB
4-14	VSWR	UHF		2		dB
4-15	IF Rejection	UHF	45	50		dB
4-16	Image Rejection	UHF	35	40		dB
4-17	RF input oscillator leakage	<890 MHz <1800 MHz			46 46	dBuV dBuV
4-18	Phase noise offset 1KHz offset 10KHz offset 100KHz	UHF UHF UHF		-58 -75 -95		dBc/Hz dBc/Hz dBc/Hz
4-19	1% cross modulation input Channel +/-2Channel level 60dBuV	UHF VHF HIGH	80 80			dBuV dBuV

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NO.	ITEM	CONDITION	MIN.	TYP.	MAX.	NOTES.
5.0	Electrical Characteristics Control refer to LGS-8GL5-A1 data sheet					
5.1	C/N in AWGN	4K 64QAM GI:1/9 FEC:0.6		16.8		dB
	8MHz,G1/4,RF=50dBm	4K QPSK GI:1/9 FEC:0.4		2		dB
	RS uncorrected error=0					
5.2	Sensitivity in AWGN	4K 64QAM GI:1/9 FEC:0.6		-81		dBm
	8MHz,GI=1/4	4K QPSK GI:1/9 FEC:0.4		-97		dBm
	RS uncorrected error=0					

8MHz CHANNEL BANDWIDTH

SUB-CARRIER MODULATION	FEC	GUARD INTERVAL Symbols	Time	PAYLOAD RATE	MPEG packets per minuteframe
4NR	0.8	945	125 us	4.812.800 bps	
		595	78.7 us	5.197.824 bps	
		420	56.56 us	5.414.400 bps	
4QAM	0.4	945	125 us	4,812,800 bps	
		595	78.7 us	5.197.824 bps	
		420	55.56 us	5,414,400 bps	
	0.6	945	125 us	7,219,200 bps	
		595	78.7 ud	7.796.736 bps	
		420	55.56 us	8,121,600 bps	
	0.8	945	125 us	9,625,600 bps	
		595	78.7 us	10.395.648 bps	
		420	55.56 us	10,828,800 bps	
16QAM	0.4	945	125 us	9,625,600 bps	
		595	78.7 us	10.395.648 bps	
		420	55.56 us	10,828,800 bps	
	0.6	945	125 us	14,438,400 bps	
		595	78.7 us	10.395.648 bps	
		420	55.56 us	16,243,200 bps	
	0.8	945	125 us	19,251,200 bps	
		595	78.7 us	20.791.296 bps	
		420	55.56 us	21,657,600 bps	
32QAM	0.8	945	125 us	24.064.000 bps	
		595	78.7 us	25.989.120 bps	
		420	56.56 us	27.072.000 bps	
64QAM	0.4	945	125 us	14,438,400 bps	
		595	78.7 us	15.593.472 bps	
		420	55.56 us	16,243,200 bps	
	0.6	945	125 us	21,657,600 bps	
		595	78.7 us	23.390.208 bps	
		420	55.56 us	24,364,800 bps	
	0.8	945	125 us	28,876,800 bps	
		595	78.7 us	31.186.944 bps	
		420	55.56 us	32,486,400 bps	

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Notice:

To gain good sensitivity under 64QAM, FEC:0.8

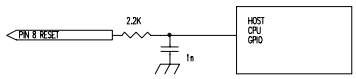
please supply PIN 4, B2 5V respectively; Please do not share voltage with other system.

PIN 1 (TU) is for engineering test purpose.

For regular application, please do not connect.

PIN 8 (RESET) has IF output for engineering tuning purpose.

For regular application, please connect 2.2K resistor near PIN 8 and 1nF capacitor to ground.



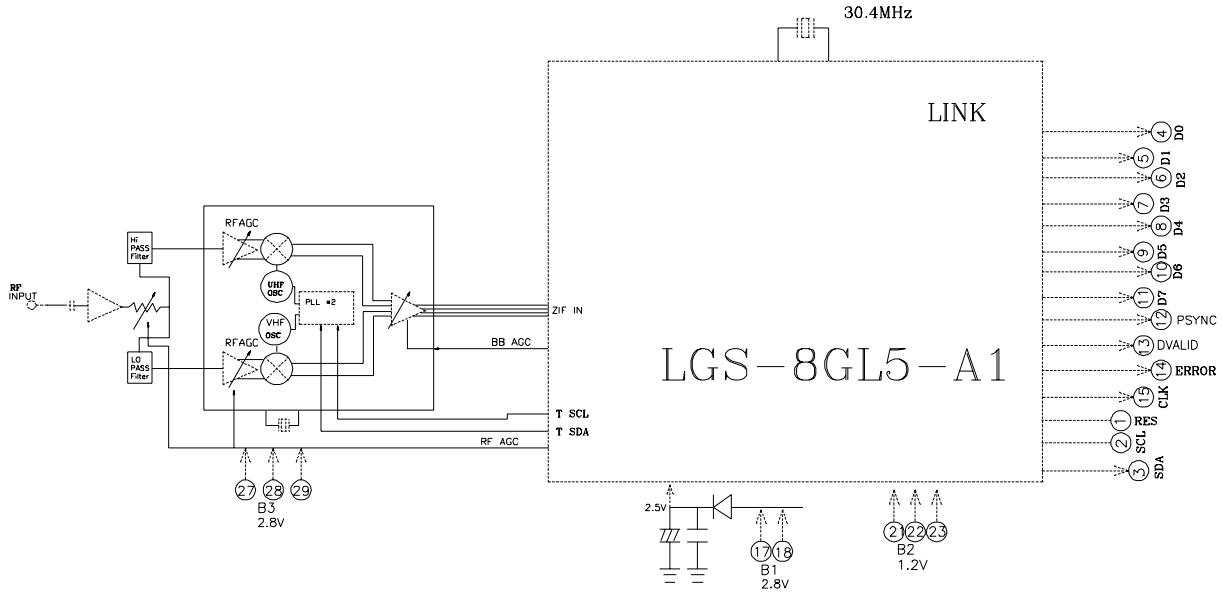
PIN 2 (ANT B+), for regular application, please do not connect.

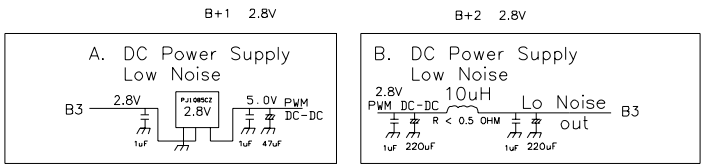
If there is ANT (ANT + RF AMP), please supply proper voltage to ANT.

Notice:The current should not be over 100mA.

To prevent ANT DC short, current protection circuit is necessary if PIN 2 is supplied with voltage.

PCB circuit will be burned out if the current is over 300mA.





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5. TUNER PLL PROGRAMMING

TABLE 8-4 BIT Read/Write

ADDRESS Btye	1	1	0	0	0	MA1	MA0	0	A	BYET1
Divider Byte1	0	14 2	13 2	12 2	11 2	10 2	9 2	8 2	A	BYTE2
Divider Byte2	7 2	6 2	5 2	4 2	3 2	2 2	1 2	0 2	A	BYTE3
Control byte	1	CP	T2	T1	T0	RSA	RSB	OS	A	BYTE4
Bandswitch Byte	0	0	0	P4	P3	P2	P1	P0	A	BYTE5
AGC Control Byte*	ATC	AL2	AL1	AL0	0	0	0	0	A	BYTE6

* Byte6 replaces byte5 when T2,T1,T0=0,1,1

ADDRESS	1	1	0	0	0	MA1	MA0	1	A	BYTE1
STATUS BYTE	POR	FL	1	1	AGC	A2	A1	A0	A	BYTE2

A:ACKNOWLEDGE BIT.

MA1,MA0:VOLTAGE ADDRESS BITS.(Fix MA1,MA0=0,0)

CP:charge pump current bits bit=0 50uA or 125uA

bit=1 250uA(default)or 650uA

see table 8-11 charge pump current

T0,T1,T2:test bits.see table 8-7 test modes

RSA,RSB:reference divider bits see table 8-8 reference divider

OS:tuning control bit bit=0 enable Vt

bit=1 disable Vt

P0,P1,P2,P3:VHFLO,VHFHI,UHF,BANDSWITCH AND ANT SWITCH see table 8-12

P4:NPN port control bit bit=0(fix AGC Voltage input)

ATC:AGC timer constant bit bit=0 time 2S

bit=1 time 50ms

AL0,AL1,AL2:AGC take-over point bits,see table 8-9

POR:power-on reset flag:POR=0 AT POWER-ON

FL:PHASE LOCK DETECT FLAG.bit=1 OSC LOCK

bit=0 OSC UNLOCK

AGC:internal AGC .fiag AGC=1 when internal AGC is active (level below 3V)

A0,A1,A2:5-level AGC Voltage

TABLE 8-7 Test modes	T2	T1	T0
Normal mode, charge pump currents 50 and 250uA selectable	0	0	0
Normal mode, charge pump currents 50 and 250uA selectable(default)	0	0	1
CP is in high-impedance state	0	1	0
Byte6 will follow(otherwise byte5 will follow)	0	1	1
P0=Fdiv OUTPUT ,P1=Fref OUTPUT	1	0	0
not in use	1	0	1
Extended mode charge pump currents 50 and 250uA selectable	1	1	0
Extended mode charge pump currents 125 and 650uA selectable	1	1	1

TABLE 8-8 Reference divider ratios

Reference divider ratios	PLL 4MHz quartz	Mode	T2	T1	REA	RSB
80	50KHz	normal	0	0	0	0
128	31.25KHz	normal	0	0	0	1
24	166.67KHz	X	X	X	1	0
64	62.5KHz	X	X	X	1	1
32	125KHz	extended	1	1	0	0
28	142.86KHz	extended	1	1	0	1

TABLE 8-9 AGC Take-over point

IF output level symmetrical mode	A2	A1	A0
118 dBuV	0	0	0
115 dBuV	0	0	1
112 dBuV	0	1	0
109 dBuV	0	1	1
106 dBuV	1	0	0
103 dBuV	1	0	1

TABLE 8-11 charge pump current

Charge pump current	mode	CP	T2	T1	T0
50uA	normal	0	0	0	x
250uA	normal	0	0	0	x
50uA 174~349 MHz 428.1~659 MHz	extended	0	1	1	0
125uA 349.1~397 MHz 659.1~759 MHz	extended	0	1	1	1
250uA 397.1~428 MHz 759.1~862 MHz	extended	1	1	1	0
650uA	extended	1	1	1	1

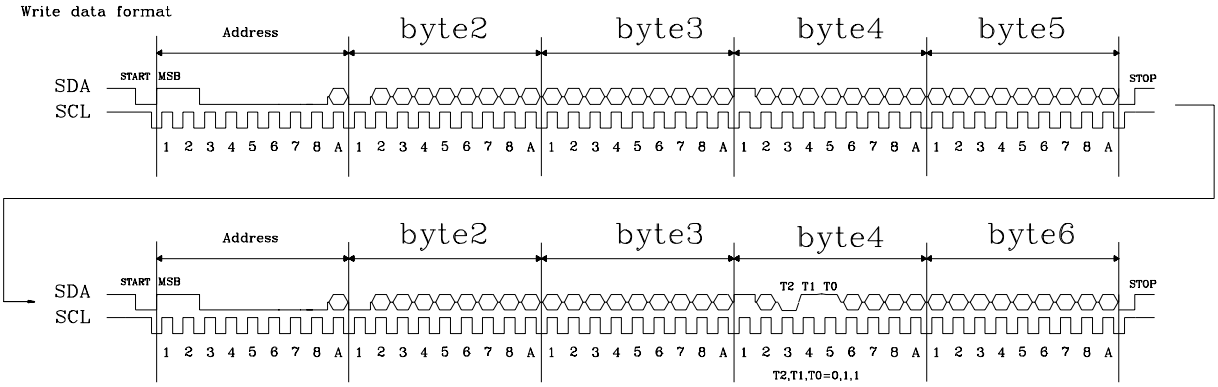
note :x=don't care.

Analog signal charge pump=50uA ,Digital signal charge=50uA~250uA

TABLE 8-12 3-band selection and B/W switch

	P0	P1	P3	P2
UHF	0	0	1	X

I2C BUS Timing Diagram and telegram examples



6. **Electorstic discharge**

6.1 **Test**

Each front-end must be capable of normal performance following its subjection to the following tests:

MIL STD 883C HBM

Test is performed with a voltage discharge from a 100 **PF** capacitor over a 1500 **OHM** series resistance in the discharge path. There is a direct contact between the test probe head and the unit under test, using the test points and conditions detailed below:

- Test to pins 1 through 22:
  3 successive ESD discharges of **+/-2 KVDC** between each pin and the front-end frame.

IEC 1000-4-2

Test is performed with a voltage discharge from a 150 **PF** capacitor over a 330 **OHM** series resistance in the discharge path. There is a direct contact between the test probe head and the unit under test, using the test points and conditions detailed below:

- Test for antenna input socket +/-8 **KVDC**
- Test for antenna output socket +/-5 **KVDC**

6.2 **Handling**

Anyone handling a front-end must wear a properly grounded anti-static discharge bracelet to minimize **ESD** damage.
After each front-end is aligned and tested, it will be packed with anti-static material prior to transportation and storage. This package is to remain in place until the front-end is assembled and soldered onto the receiver main board.

7 **Reliability test procedure & conditions**

Note:Room temperature = 25°C +/- 2°C

7.1 **Heat load test**

- o Measure the DUTs at room temperature
- o Load the DUTs into chamber of the following conditions:

Temperature	=	60 °C
Period	=	500 hrs
Cycle	=	1.5 hrs on; 0.5 hrs off
Quantity	=	10 pcs

- o Cool-down 0.5 hr at room temperature, then measured the DUTs within 1 hr
- o The test shall be continued to 1000 cycles for information only

7.2 **Humidity load test**

- o Measure the DUTs at room temperature
- o Load the DUTs into chamber of the following conditions:

Temperature	=	40 +/- 5 °C
Period	=	24 hrs
Cycle	=	constantly on
Quantity	=	24 pcs

- o Cool-down 0.5 hr at room temperature, then measured the DUTs within 1 hr
- o Load the DUTs again into chamber of the following conditions:

Temperature	=	40+/-5°C
Humidity	=	90 to 95%
Period	=	500 hrs
Cycle	=	1.5 hrs on; 0.5 hr off
Quantity	=	20 pcs

- o Cool down 0.5hr at room temperature, then measured the DUTs within 1 hr

7.3 **Cold test**

- o Measure the DUTs at room temperature
- o Load the DUTs into chamber of the following conditions:

Temperature = -2 +/-5 °C
Period = 500 hrs
Cycle = constantly on
Quantity = 10 pcs

- o Warm up for 2 hrs at room temperature, then measured the DUTs within 1 hr

7.4 **Thermal shock**

- o Measure the DUTs at room temperature
- o Load the DUTs into chamber of the following conditions:

Temperature = -25°C for 60 min
↓ ↑
80°C for 60 min
Period = 200 cycles
Power = power off
Quantity = 10 pcs

- o Cool-down 0.5 hr at room temperature then measured the DUTs within 1 hr

7.5 **Temperature cycle test**

- o Measure the DUTs at room temperature
- o Load the DUTs into chamber of the following conditions:

Temperature = -5°C for 16 hrs then 60°C for 8 hrs
Period = 500 hrs
Cycle = constantly on
Quantity = 10pcs

- o Cool down 0.5 hr at room temperature, then measured the DUTs within 1 hr
- o Load the DUTs again into chamber of the following conditions:

Temperature = 40 +/- 5°C
Humidity = 90 to 95%
Period = 500 hrs
Cycle = 1.5 hrs on; 0.5 hrs off
Quantity = 10 pcs

- o Cool down 0.5 hr at room temperature, then measured the DUTs within 1hr

7.6 **Vibration test**

- o Frequency: 3.5 Hz
- o Vertical amplitude: 15 to 25 mm
- o Duration: 1 hr
- o Quantity: 1 carton

7.7 **Drop test**

- o Packaged apparatus: <or = 50 kg
- o Height: depend on weight
- o 1 corner + 3 edge + 6 faces

Drop on the weakest corner (point G)
Drop on the shortest edge on contact with point G
Drop on average edge in contact with point G
Drop on the longest edge in contact with point G
Drop flat wise on the side of minimum surface
Drop flat wise on the side of opposite minimum surface
Drop flat wise on the side of average surface
Drop flat wise on the side of opposite average surface
Drop flat wise on the side of maximum surface
Drop flat wise on the side of opposite maximum surface

- o Quantity :1 carton

7.8 Life test

- o Measure the DUTs at room temperature
- o Load the DUTs into chamber of the following conditions:

Temperature = 60 °C
Period = 500 hrs
Cycle = constantly on
Quantity = 20 pcs

- o Cool down 0.5 hr at room temperature, then measure the DUTs within 1hr

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Pin No	Connection
1	RES
2	SCL
3	SDA
4	D0
5	D1
6	D2
7	D3
8	D4
9	D5
10	D6
11	D7
12	PSYNC
13	DVALID
14	ERROR
15	CLK

Pin No	Connection
16	GND
17	B1(2.8V)
18	B1(2.8V)
19	GND
20	GND
21	B2(1.2V)
22	B2(1.2V)
23	B2(1.2V)
24	GND
25	GND
26	GND
27	B3(2.8V)
28	B3(2.8V)
29	B3(2.8V)
30	GND

PIN NO. LIST
1 RES Demodulator REST(to Lo REST)
2 SCL I2C CLOCK
3 SDA I2C DATA
4~11 D0~D7 BIT DATA OUT
12 PSYNC
13 DVALID
14 ERROR DATA ERROR SIGNAL
15 CLK BIT CLOCK OUT
16 GND
17~18 B1 2.8V Demodulator B+
19~20 GND
21~23 B2 1.2V Demodulator B+
24~26 GND
27~29 B3 2.8V ZIF & A/D B+
30 GND

NOTE 1.TOLERANCES ARE ±0.5.
UNLESS OTHERWISE SPECIFIED.