SPECIFICATION

DVBT TUNER

1.SCOPE

The MDVBT-7K8 is intended for the reception of DVB-T compliant MPEG2 signals (full TES 300 744 compliant) in combination with the tuner ,all functions are integrated to deliver a corrected stream given DVB-T encoded signal(2k or 8k mode)with 7MHz or 8MHz bandwidth.

2.GENERAL SPECIFICATIONS

2-1. RECEIVING FREQUENCY RANGE	VHF HI 177.5~226.5MHz	
	UHF 474~862MHz	
2-2. SUPPLY VOLTAGE	:B1,	5V +/-2%
	B2	5V +/-2%
	B3	1.8V +/-2%
	B4	3.3V +/-2%
2-3. CONSUMPTION CURRENT	:B1	5V 110 mA
	B2	5V 30 mA
	B3	1.8V 180 mA
	B4	3.3V 3 mA

Pin 2 Ant Power is for active Ant. The maximum current shall not exceed 100mA.
To avoid destroying the components inside the tuner,please offer current limited circuit if you need to supply Pin 2 with current.

2-4. OPERATION AND STORAGE CONDITIONS FOR GUARANTEE	TEMPERATURE 0~50^{O}C
	HUMIDITY 85% OR LESS

3.TEST CONDITIONS

3-1. TESTING AMBIENT CONDITIONS
DEFINED AS TEMPERATURE OF 25+/-2^{O}C AND HUMIDITY OF 65+/-5% RH.
NOTE : THAT TEMPERATURES OF 5~30^{O}C AND HUMIDITY OF 45~85% MAY BE REGARDED AS STANDARD.

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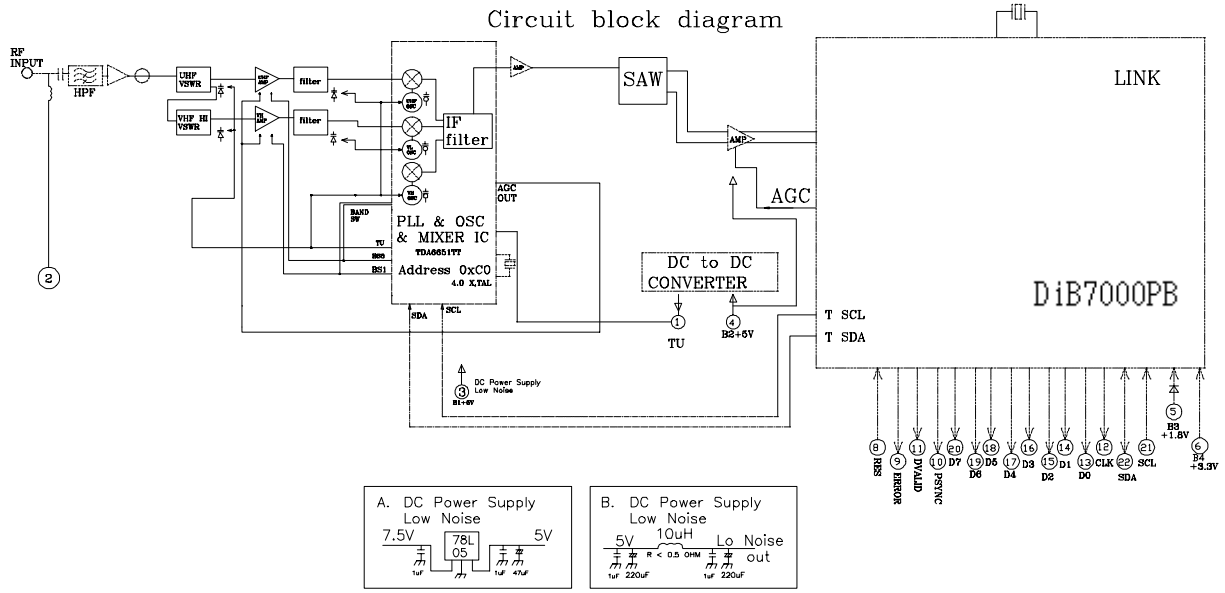
NO	ITEM	CONDITION	MIN	TYP	MAX	NOTES
1.	GENERAL SPECIFICATIONS					
1.1	Receiving frequency range	UHF SEE Page 8	474		862	MHz
		VHF HIGH SEE Page 8	177.5		226.5	
1.2	Mergin frequency	UHF	-6		+3	MHz
		VHF HIGH	-5		+2	
1.3	RF input impedance	F CONNECTOR 75 OHM				
1.5	L.O PLL synthesizer IC	TDA6651TT Address 0xC0				
1.6	PLL synthesizer crystal	+/- 50 ppm		4.0		MHz
1.7	1st intermediate frequency	DVB-T		36.167		MHz
	3dB BW			8		MHz
1.10	AGC voltage input external	0V to 5V 0V min gain				Current
		5V max gain				20uA max
2	Operating Voltage	Supply voltage 5V +/- 2% 3.3V +/- 2% 1.8 +/- 2%				
2.2	Humidity	Operating less than 85%				
		Storage less than 95%				
2.3	Temperature	Operation 0°C to 50°C				
		Storage -20°C to 75°C%				

Circuit block diagram



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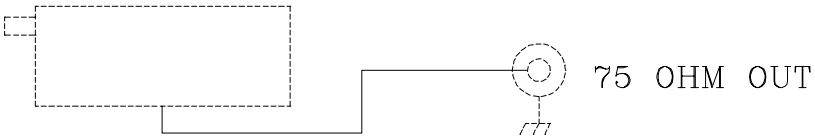
NO.	ITEM	CONDITION	MIN.	TYP.	MAX.	NOTES
	TEST CONDITION					
3.	Supply voltage Ambient humidity Ambient temperature	B1, +5V B2+1.8V B3+3.3V 60% to 70% 20°C to 30°C				
3.1	Test circuit					
3.2	Noise Figure	UHF VHF HIGH		7 6	10 9	dB dB
3.3	AGC Range AGC voltage 5V to 0.5V	UHF VHF HIGH	35 40	55 65		dB dB
3.5	Gain taper				8	dB
3.6	VSWR	UHF VHF HIGH VHF LOW		2 2 2		dB dB dB
3.7	IF Rejection	UHF VHF HIGH	45 45	50 50		dB dB
3.8	Image Rejection	UHF VHF HIGH	40 30	50 40		dB dB
3.9	RF input oscillator leakage	<890 MHz <1800 MHz			46 46	dBuV dBuV
3.10	Phase noise offset 1KHz offset 10KHz offset 100KHz	UHF VHF HIGH UHF VHF HIGH UHF VHF HIGH		-58 -60 -75 -75 -95 -95		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
3.2	1% cross modulation input Channel +/-2Channel level 60dBuV	UHF VHF HIGH	80 80			dBuV dBuV

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NO.	ITEM	CNODITION	MIN.	TYP.	MAX.	NOTES.
5.0	Electrical Characteristics Control refer to DiB7000PB data sheet					
5.1	C/N in AWGN	8K 64QAM R7/8		22.5		dB
	8MHz,G1/4,RF=50dBm	8K 64QAM R2/3		18.7		dB
	RS uncorrected error=0	8K 64QAM R1/2		16.5		dB
		8K 16QAM R3/4		14.6		dB
		8K 16QAM R2/3		13.1		dB
		8K QPSK R1/2		5.1		dB
5.2	Sensitivity in AWGN	8K 64QAM R7/8		-72		dBm
	8MHz,GI=1/4	8K 64QAM R2/3		-76		dBm
	RS uncorrected error=0	8K 64QAM R1/2		-80		dBm
		8K 16QAM R3/4		-81		dBm
		8K 16QAM R2/3		-84		dBm
		8K QPSK R1/2		-91		dBm
5.3	C/N in 0dB Echo	8K 64QAM R3/4		27.6		dB
	8MHz,658MHz,G1/4,RF=-50dBm	8K 64QAM R2/3		23.2		dB
	Crition:Picture Quality					
5.4	Echo Outside Guard Interval	8K 64QAM R=3/4 GI=1/4 -/+260uS		15		dB(PATH LOSS)
	RS uncorrected error=0	8K 64QAM R=2/3 GI=1/8 -/+260uS		12		dB(PATH LOSS)
	8MHz,658MHz,RF=-50dBm					
5.5	Frequency Offset	8K,8MHz,64QAM,R2/3, G1/8,-60dBm	-200		+200	KHz
5.6	Immunity to Digital ACI	8K,64QAM,R=3/4,GI=1/4(N+/-1)		28		dB
	8MHz,658MHz	8K,64QAM,R=2/3,GI=1/8(N+/-1)		28		dB
	RS uncorrected error=0					
5.7	Mobile Performance	2K,16QAM,R=3/4,GI=1/3		300		km/h
	RF Levekl=-50dBm,658MHz	8K,64QAM,R=1/2,GI=1/4		105		km/h
	8MHz,C/N=OFF	8K,64QAM,R=2/3,GI=1/4		80		km/h
	Average Packet Error Rate $<5x10^{-3}$					

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6.0 Programming of tuner PLL

The tuner control (frequency selection and band switching) is done via the I²C bus.
One address byte and four data bytes are needed to fully program the tuner.
A PLL lock flag can be read from the tuner during 'READ'-mode.

I²C-bus data format, 'WRITE'-mode:

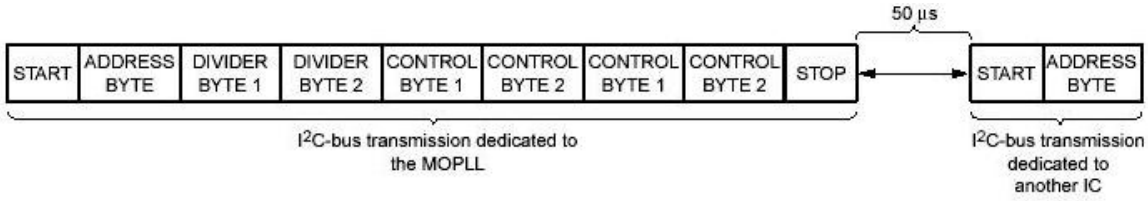
NAME	BYTE	MSB						LSB	ACK
Address byte	1	1	1	0	0	0	0	R/W=0	A
Prog.Divider Byte 1	2	0	N14	N13	N12	N11	N10	N9	N8	A
Prog.Divider Byte 2	3	N7	N6	N5	N4	N3	N2	N1	N0	A
Control Data Byte 1	4	1	D/A=1	0	0	1	R2	R2	R0	A
	4	1	D/A=0	0	0	ATC	AL2	AL1	AL0	
Control Data Byte2	5	CP2	CP1	CP0	SP5	SP4	SP3	SP2	SP1	A

A=acknowledge

Timing of program sequences:

Because of the Tuner-PLL frequency divider setting time of min. 50usec.,the occurrence of any other I²C traffic start condition present within that periode on the Bus will disturb the divider and result in a not peoperly tuned tuner VCO.
Each time the Tuner-PLL frequency divider has been programmed, a 50usec wait becomes necessary before continuing the I²C bus traffic.

Following table demonstrates a correct program sequence:



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Description of used symbols:

R/W	:Read / Write bit ; Bit = 0 => Write mode Bit = 1 => Read mode
N14 to N0	:LO frequency divider bits
D/A	:D/A = 1 => follwing 6 bits contain test and reference divider ratio data :D/A = 0 => follwing 6 bits contain AGC setting data
R2,R1,R0	:reference divider bits (see table:Reference Divider Settings)
ATC	:AGC time constant data bit; only valid with int.AGC loop active ATC = 1 => enables fast tuning speed during channel search mode ATC = 0 => recommended after channel acquisition;nomal mode
AL2,AL1,AL0	:AGC Take-Over-Point bits (see table:Internal AGC loop TOP)
CP2,CP1,CP0	:PLL charge pump current selection bits(see table:Charge Pump Settings)
SP5.....SP1	:Switch ports; bit = 1 => port V_{out} is 'ON' bit = 0 => port V_{out} is 'OFF' (see table:Band and SAW-filter selection table)

N14 to N0: programmable divider bits

divider ratio: $N=N14x2^{14}+N13x2^{13}+...+N1x2^{1}+N0$

How to calculate the divider ratio N :

$$N=\frac{(f_{input}+f_{IF}}{f_{ref}}\left[\frac{Hz}{Hz}\right] \text{ whereby } f_{ref}=\frac{4x10^6}{64^{(1)}}\ [Hz]=62.5kHz$$

$$f_{ref}=\frac{4x10^6}{24^{(1)}}\ [Hz]=166.6\overline{7}kHz$$

Note(1):divider ratio to be set with Bits;R2...R0'(see table below)

Do not set the divider ratio as such that the tuner is tuned into extreme conditions i.e.far below or far above the specified ranges.

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R2,R1,R1: PLL reference divider settings (Control Data Byte 1):

PLL step size	PLL ref. divider ratio	R2	R1	R0
50.0kHz	80	0	1	1
62.5kHz	64	0	0	0
166.67kHz	24	0	1	0

AL2,AL1,AL0: AGC Take-Over-Point bits(Control Data Byte 1):

AL2	AL1	AL0	Typical TOP Level	Remarks
0	0	0	TOP = 124dBuVpp	
0	0	1	TOP = 121dBuVpp	
0	1	0	TOP = 118dBuVpp	
0	1	1	TOP = 115dBuVpp	
1	0	0	TOP = 112dBuVpp	
1	0	1	TOP = 109dBuVpp	
1	1	0	I_{AGC} = 0	External AGC(1)
1	1	1	V_{AGC} = 3.5V	Loop disabled(2)

Note 1: The tuner internal AGC current sources are disabled (default mode after power on reset).

Note 2: The tuner internal AGC detector is disable. With no external AGC voltage applied to the tuner, the RF-gain is always set to maximum.

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CP2,CP1,CP0:PLLcharge pump current settings

Note: during search tuning it is recommended to set the PLL to a moderate charge pump.
To enable best oscillator phase nosie performance during digital signal processing,
the PLL charge pump current should be set to conditions as given with following table.

In analog applications the PLL charge pump current must be set to max. 60uA !

CP2	CP1	CP0	Typical CP current	Recommendations
0	0	0	40 uA	
0	0	1	60 uA	
0	1	0	90 uA	**To be used during search tuning and for 50 kHz, 62 kHz PLL step sizes**
0	1	1	130 uA	VH : 161MHz - 254MHz U : 446.1MHz - 584MHz
1	0	0	190 uA	
1	0	1	280 uA	VH : 254.1MHz - 384MHz U : 584.1MHz - 794MHz
1	1	0	410 uA	VH : >384.1MHz U : >794.1MHz

SP5...SP1:Band selection table

	SP5	SP4	SP3	SP2	SP1
VHF Hi band	X	X	0	0	1
UHF band	X	X	1	0	0

I²C- bus data format, 'RADE' - mode:

Name	MSB							LSB	
Address byte	1	1	0	0	0	0	0	R/W=1	A
Status byte	POR	FL	0	1	AGC	1	0	0	A

A : Acknowledge

POR = power-on-reset-flag ; POR = 1 on power-on

FL = in-lock-flag ; FL = 1 when PLL is phase locked

AGC = internal AGC flag ; AGC = 1 when internal AGC is active

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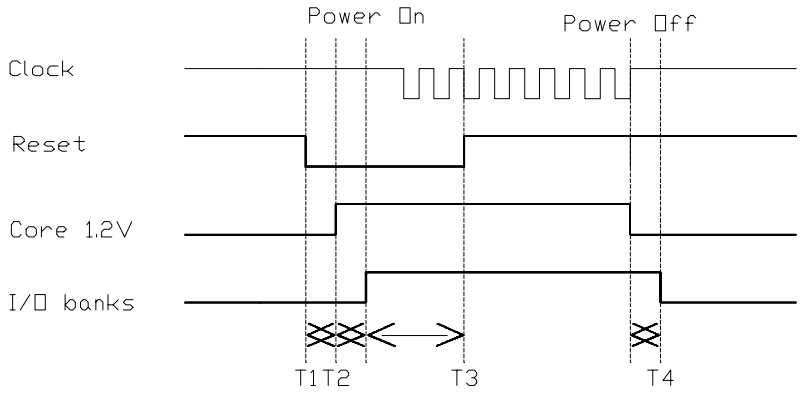

power on and off sequence

1. DiB IC can support I2C clock up to 1MHZ

2. After reset release,you can send immediatly I2C messages.Maybe wait 1-2 clock cycle before sending I2C message,just to be sure.

3. The only limit is T3 > 10ms.

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