SPECIFICATION

DVBS TUNER Revision:1.0

1.SCOPE

Jdvbs-90502 series is RF unit for Japan digital Bs/cs satellite broadcast reception.
Built OFDM demodulator IC.

CH VS. IF

ISDB-S		DVB-S	
CH	IF	CH	IF
BS-1	1049.48	JD1	1308.00
BS-3	1087.84	JD3	1338.00
BS-5	1126.20	JD5	1368.00
BS-7	1164.56	JD7	1398.00
BS-9	1202.92	JD9	1428.00
BS-11	1241.28	JD11	1458.00
BS-13	1279.64	JD13	1488.00
BS-15	1318.00	JD15	1518.00
BS-17	1356.36	JD17	1068.00
BS-19	1394.72	JD19	1108.00
BS-21	1433.08	JD21	1148.00
BS-23	1471.44	JD23	1188.00
		JD25	1228.00
		JD27	1268.00

2.GENERAL SPECIFICATIONS

2-1 Receiving Frequency : 950~2150 MHz
2-2 RF Input Impedance : 75 OHM
2-3 Lo PLL Synthesizer IC : Built in PLL
(IC Bus: CE5037)
2-4 RF Input Connector : F Type (Female)
2-5 PLL Step Size : 1MHz
2-6 Operating Voltage 1)Supply voltage for Tuner IC : B3, 3.3V
2)Supply voltage for DMIC : B1, 1.5V
; B2, 2.5V
; B3, 3.3V

2-7 Temperature Range
Storage Temperature : -20°C ~ + 80°C
Operation Temperature : 0°C ~ + 50°C

3.TEST CONDITIONS

3-1. Test conditions : All data held under following conditions
: +25+/-2°C / Humidity : 45 ~ 65% RH

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4.ELECTRICAL SPECIFICATION OF THE RF TUNER

Test Condition

1.Supply Voltage
- 1-1 Supply Voltage (B1) :1.5V +/- 0.1V DC
- 1-2 Supply Voltage (B2) :2.5V +/- 0.1V DC
- 1-3 Supply Voltage (B3) :3.3V +/- 0.1V DC

2.Ambient Temperature :25°C +/- 5°C

3.Ambient Humidity :65% +/- 10%

Current Consumption

Pin No.	Parameter	Min.	Typ.	Max.
3	B1 1.5V(DVBS)		186mA	
	B1 1.5V(ISDBS)		186mA	
5	B2 2.5V(DVBS)		86mA	
	B2 2.5V(ISDBS)		86mA	
6	B3 3.3V(DVBS)		148mA	
	B3 3.3V(ISDBS)		140mA	

Characteristic	Min.	Typ.	Max.	Units.	Conditions
Input Return Loss		9		dB	Zo = 75 ohm with external matching. Bypass enabled or disabled
Noise Figure DSB		8	10	dB	At max gain
		8.5	10	dB	At -70 dBm operating level
			13	dB	At -60 dBm operating level
Variation in NF with RF gain adjust			-1	dB/dB	Above -60 dBm operating level
Operating dynamic range		-92	-10	dBm	1 MS/s
Operating dynamic range		-84	-10	dBm	27.5 MS/s
Conversion Gain					
Max	72	78		dB	RFagc = 0.2 V
Min		-6	10	dB	RFagc = 2.8 V
AGC Control Range	68	72		dB	AGC monotonic for RFagc from Vee to Vcc
RFAGC input current	-150		150	uA	Vee < = RFagc < = Vcc
System IM2			-28	dBc	Baseband defined, note 1
			-40	dBc	RF front-end defined, note 2
System IM3			-24	dBc	Note 3
			-30	dBc	Note 4
IIP2	15	22		dBm	At -40 dBm input, note2
IIP3	5	13		dBm	At -25 dBm input, note3

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Characteristic	Min.	Typ.	Max.	Units.	Conditions
LO second harmonic interference level			-35	dBc	Note 5, all gain setting
LNA second harmonic interference level			-20	dBc	Note 6
Quadrature gain match	-1		1	dB	1.5 to 18 MHz
Quadrature phase match	-3 -5		3 5	deg deg	Baseband Signal = 1.5 MHz Baseband Signal = 18 MHz
I & Q channel in band ripple			1	dB	1.5 to 18 MHz
LO reference sideband spur level on I & Q outputs			-40	dBc	synthesizer phase detector comparison frequency 500 - 2000 kHz
In band local oscillator leakage to RF input			-65 -55	dBm dBm	950 - 2150 MHz 30 - 950 MHz
Channel lock time			50	ms	Worst case channels
Local Oscillator					
VCO Gain		27		MHz/V	LO = 2GHz. Note 7
SSB Phase Noise		-83	-76 -96 -100	dBc/Hz dBc/Hz dBc/Hz	10kHz offset 100 kHz offset 1 MHz offset
Phase Noise floor			-132	dBc/Hz	
Integrated phase litter			3	deg	10 kHz to 15 MHz
Varactor input current	-10		10	nA	Vvar = 0.5 to 1.3 V
Baseband Filters					
Bandwidth	6		43	MHz	Max specified load
Bandwidth Tolerance	-1		+1	MHz	All bandwidth settings
Time to change filter			10	ms	
bandwidth					
Total Harmonic Distortion			-30	dBc	1 Vpp differential output at 43 MHz filter Bandwidth
RF Bypass					Output load = 75 ohms
Gain	-2	1.5	4	dB	
Noise Figure		8.5	10	dB	
OPIP 3		9		dB	Note 8
OPIP 2	20			dBm	Note 9
Output return loss	9			dB	
Forward Isolation		30		dB	950-2150 MHz. Bypass disabled
Reverse Isolation		30		dB	950-2150 MHz. Bypass enabled or disabled
In band LO leakage			-65	dBm	950-2150 MHz. Bypass enabled or disabled.

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Characteristic	Min.	Typ.	Max.	Units.	Conditions
Synthesizer					
Charge Pump Current	304 422 578 762	400 550 750 1000	552 759 1035 1380	uA uA uA uA	
Charge Pump Matching		2		%	Vpin = 0.5 to 1.3 V
Charge Pump Leakage	-10	+/-3	+10	nA	Vpin = 0.5 to 1.3 V
Charge Pump Compliance	0.4		Vcc -0.4	V	
Crystal Frequency	4		20	MHz	
Recommended Crystal series resistance	12	25	50	ohm	10 MHz crystal
Crystal power dissipation		100	500	uW	Note 10
Crystal load capacitance		16		pF	Note 10
Crystal oscillator startup time			10	ms	
External reference input frequency	4		20	MHz	ac coupled sinewave
External reference drive level	0.5		2.0	Vpp	ac coupled sinewave
Phase detector comparison frequency	0.5		2	MHz	
Equivalent phase noise at phase detector		-148		dBc/Hz	10 MHz crystal SSB within PLL loop bandwidth
Interface					
SDA, SDL Input high voltage Input low voltage Hysteresis Input current	 2.3 0 -10	 0.4 	 3.6 1 10	 V V uA	 Input = Vee to VccDIG +0.3 V
SDA Output Voltage			0.4	V	Isink = 3 mA
SCL clock rate			100	kHz	
External Port P0 Sink Current Leakage Current	 3 	 	 10	 mA uA	 Vo = 0.7 V Vo = Vcc
SLEEP Input Input high voltage Input low voltage Input Current	 1.9 Vee 	 	 3.6 1.0 10	 V V uA	 Vin = Vee to VccDIG

Note 1: AGC set to deilver an output of 0.5Vp-p with an input CW @ frequency fc of -30 dBm, undesired tones ar fc +146 and fc +155 MHz @ -15 dBm, generating output IM spur at 9 MHz. Measured relative to unwanted signal.

Note 2: LO set to 2145 MHz and AGC set to deliver a 5 MHz output of 0.5Vp-p with an input CW @ frequency 2150 MHz of -40 dBm. Undesired tones at 1.05 and 1.1 GHz at -25 dBm generating IM spur at 5 MHz baseband. Measured relative to unwanted signal.

Note 3: AGC set to deliver an output of 0.5Vp-p with an input CW @ frequency fc of -30 dBm. Two undesired tones at fc+205 and fc+405 MHz at-12 dBm, generating output IM spur at 5 MHz.

Note 4: AGC set to deliver an output of 0.5Vp-p with an input CW @ frequency fc of -30 dBm. Two undesired tines at fc+55 and fc+105 MHz at -15 dBm, generating output IM spur at 5 MHz.

Note 5: The level of 2.01 GHz down converted to baseband relative to 1.01 GHz with the oscillator tuned to 1 GHz.

Note 6: The level of second harmonic of 1.01 GHz at -20dBm downconverted to baseband relative to 2.01 GHz desired signal at -35dBm with agc set to get 0.5Vp-p output. LO frequency = 2 GHz.

Note 7: Reference VCO gain value for loop filter calculations. Using this recommended value then takes into account VCO switching and automatic charge pump current variations.

Note 8: Two input tones at fc+50 and fc+100 MHz at -12dBm, generating output IM product at fc.

Note 9: IM2 product from two input tones at 1.05 and 1.1 GHz at -16 dBm, generating IM product at 2150 MHz.

Note 10: Crystal specifications vary considerably and significantly effect the choice of external oscillator capacitor values. Each application may require separate consideration for optimum performance.

2.0 Register Map and Programming

The register map is arranged as 16 byte-wide read/write registers grouped by functional block. The registers may be written to and read-back from either sequentially (for lowest overhead) or specifically (for maximum flexibility).

A significant number of bits are used for test and evaluation purposes only and are fixed at logic '0' or '1'. The correct programming for these test bits is shown in the table below. It is essential that these values are programmed for correct operation. When the contents of the registers are read back the value of some bits may have changed from their programmed value. This is due to the internal automatic control which can update registers. Any changes can be ignored.

Read only bits are marked with an asterisk(*). Any data written to these bits will be ignored.

Registers are set to default settings on applying power. These conditions are shown below and in the applicable tables.

Register	Block	Function							
0	PLL	PLF	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
1	PLL	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
2	PLL	0	0	C1	C2	R3	R2	R1	R0
3	PLL	X*	1	0	0	0	0	0	0
4	RF Front End	X*	1	1	0	1	1	LEN	RFG
5	Base Band	BF7	BF6	BF5	BF4	BF3	BF2	BF1	BF0
6	Base Band	0	LF	SF	BR4	BR3	BR2	BR1	BR0
7	Base Band	BLF*	BG3	BG2	BG1	BG	0	0	0
8	Local Oscillator	ELF*	0	1	0	0	0	0	0
9	Local Oscillator	1	0	1	0	0	0	1	0
A	Local Oscillator	1	1	1	1	0	0	0	1
B	Local Oscillator	X*	X*	1	1	1	0	0	0
C	Local Oscillator	1	1	0	1	0	0	0	0
D	Local Oscillator	X*	X*	X*	1	0	0	0	0
E	Local Oscillator	X*	X*	1	1	0	0	0	0
F	General	PD	CLR	P0	0	X*	X*	X*	X*

Table 2 Register Map

X* denotes a read only test bit

2.1 PLL Register

There are four registers that control the PLL:

Bit Field	Name	Default	Type	Description
7	PLF	-	R	PLL Lock Flag
6:0	$2^{[14:8]}$	0	R/W	MSB bits of LO Divider register

Table 3 - Register 0

The PLF bit is the PLL lock detect circuit output. The PLF bit is set after 64 consecutive comparison cycles in lock.

A chip-wide reset initializes the lock detect output to 0.

The $2^{[14:8]}$ bits are the MSB bits of the LO Divider divide value.

Bit Field	Name	Default	Type	Description
7:0	$2^{[7:0]}$	0	R/W	LSB bits of LO Divider register

Table 4 - Register 1

The $2^{[7:0]}$ bits are the LSB bits of the LO Divider divide value. The division ration ratio of the LO divider is fully programmable to integer values within the range of 240 to 32767.

Note that when the LO Divider divide value is to be changed. the new value is not actually presented to LO Divider until all of the 15-bit control word $2^{[14:0]}$ has been programmed. Register 0 and 1 must be therefore be programmed (in any order) before the LO divider is updated even if the only data change is in one of the registers.

Bit Field	Name	Default	Type	Description
7:6	-	0	R/W	Test modes
5:4	C[1:0]	0	R/W	Charge pump current
3:0	R[3:0]	0	R/W	Reference divider ratio

Table 5 - Register 2

The C[1:0] bits set the programmed charge pump current

C[1]	C[0]	Typ	Units
0	0	400	uA
0	1	550	uA
1	0	750	uA
1	1	1000	uA

Table 6 - Charge Pump Currents

The charge pump current is automatically increased to the next setting dependent on the VCO sub band that has been selected by the VCO tuning algorithm. This is to compensate for changes in VCO gain and so provide consistent PLL performance across all sub bands. Programming the highest charge pump value will not allow the value to be incremented, therefore this value should not be programmed.

The value read back for the charge pump current is the actual value in use for the selected sub band.

The R[3:0] bits select the Reference Divider divide ratio. The ratio selected is not a simple binary power-of-two value but through a lookup table, see Table 7 PLL Reference Divider Ratios.

R3	R2	R1	R0	Division Ratio
0	0	0	0	2
0	0	0	1	4
0	0	1	0	8
0	0	1	1	16
0	1	0	0	32
0	1	0	1	64
0	1	1	0	128
0	1	1	1	256
1	0	0	0	3
1	0	0	1	5
1	0	1	0	10
1	0	1	1	20
1	1	0	0	40
1	1	0	1	80
1	1	1	0	160
1	1	1	1	320

Table 7- PLL Reference Divider Ratios

Bit Field	Name	Default	Type	Description
7:0	-	0X40	R/W	Test Modes

Table 9 - Register 3

This register controls test modes within the PLL. This should be programmed with the default settings.

2.2 RF Control Regoster

A single register controls RF Programmability.

Bit Field	Name	Default	Type	Description
7	-	-	R	Test Modes
6:2	-	11011	R/W	Test Modes
1	LEN	1	R/W	Bypass Enable
0	RFG	0	R/W	RF Gain Adjust

Table 9 - Register 4

The LEN bit enables the RFBYPASS output. With this bit set, the RF Bypass is active even if 'software' or 'hardware' power down has been selected.
The RFG bit controls the gain of the second section of RF gain control. With this bit set, the RF gain is reduced by 10dB. This setting would normally used when an external LNA is being used.

2.3 Base Band Registers

There are there registers that control the Base Band:

Bit Field	Name	Default	Type	Description
7:0	BF[7:0]	0X3C	R/W	Base Band Filter Cut-Off Freqiency

Table 10 -register 5

The bots BF[7:0] control the bandwidth of the baseband filter. An automatic adjustment routine synchronizes the filter bandwidth to a reference frequency derived from the crystal.

Bit Field	Name	Default	Type	Description
7	-	0	R/W	Test Mode
6	LF	0	R/W	Baseband Filter Adjust Disable
5	SF	0	R/W	Baseband Filter Adjust Disable
4:0	BR[4:0]	1000	R/W	Base Band Reference Division Ratio

Table 11 - Register 6

The LF and SF bits disable the baseband filter adjustment. It is recommended that these bits are set after programming the filter bandwidth to prevent interactions within the circuit. These bits must be reset to enable the baseband filter bandwidth to be reprogrammed.
The BR[4:0] bits set the crystal reference divide ratio. This effectively determines the resolution setting of the baseband filters. The baseband filter settings (BF[7:0]) can be calculated from the following equation.

$$BF[7:0] = \frac{(\text{Filter bandwidth(MHz)} * 5.088 * BR[4:0])}{\text{Crystal Frequency (MHz)}} - 1$$

See section 3 Applications Information, for a typical programming example.
BR[4:0] = 0 is invalid

Bit Field	Name	Default	Type	Description
7	BLF	-	R	Base Band Lock Flag
6:3	BG[3:0]	0111	R/W	Base Band Gain Select
2:0	-	000	R/W	Test Modes

Table 11 - Register 6

The BLF bit indicates that the baseband adjustment has completed and locked.

The control bits BG[3:0] define the gain of the Base Band post-filter amplifier. The following table shows the gain note this is relative gain. The 1.5 dB gain steps enable the baseband output level to be adjusted and optimise gain distribution for different symbol rates.

BG[3]	BG[2]	BG[1]	BG[0]	Gain(dB)
0	0	0	0	0
0	0	0	1	1.5
0	0	1	0	3.0
0	1	0	0	6.0
0	1	0	1	7.5
0	1	1	0	9.0
0	1	1	1	10.5
1	0	0	0	12.0
1	0	0	1	13.5
1	0	1	0	15.0
1	0	1	1	16.5

Table 13 - BG[3:0]Control of Base Band Post Filter Gain

2.4 Local Oscillator Registers

There are seven registers that control the Local Oscillator: These are used primarily for test and evaluation by Intel Corporation. Although VCO's can be manually programmed, the user is recommended to use the default automatic settings as these provide optimum performance.

Bit Field	Name	Default	Type	Description
7	FLF	-	R	Full Lock Flag
6:3	-	0X20	R/W	Test Modes

Table 14 - Register 8

The FLF bit is the VCO tuning controller lock output and is set when PLL is locked and the automatic VCO tuning is optimised and complete.

Register 9 to Register E are for the test modes only. It is however important that these registers are programmed with the values shown.

Bit Field	Name	Default	Type	Description
7	-	0XA2	R/W	Test Modes

Table 15 - Register 9

Bit Field	Name	Default	Type	Description
7:0	-	0XF1	R/W	Test Modes

Table 16 - Register A

Bit Field	Name	Default	Type	Description
7:6	-	-	R	Test Modes (read only)
5:0	-	0X38	R/W	Test Modes

Table 17 - Register B

Bit Field	Name	Default	Type	Description
7:0	-	0XD0	R/W	Test Modes

Table 18 - Register C

Bit Field	Name	Default	Type	Description
7:5	-	-	R	Test Modes (read only)
4:0	-	0X10	R/W	Test Modes

Table 19 - Register D

Bit Field	Name	Default	Type	Description
7:6	FLF	-	R	Test Modes (read only)
5:0	-	0X30	R/W	Test Modes

Table 20 - Register E

2.5

This register control powerdown and general control functions:

Bit Field	Name	Default	Type	Description
7	PD	1	R/W	Power Down
6	CLR	0	R/W	Clear and reset logic
5	P0	0	R/W	Port 0 control
4	-	0	R/W	Test Mode
3:0	-	-	R	Test Modes (Read only)

Table 21 - Register F

The PD bit is the 'software' power down control. When this bit is set to 1, all the analogue blocks are powered down with the exception of the Crystal Oscillator. The I²C interface will remain active and can still be used to enable the RF Bypass.

Setting the SLEEP input pin high also invokes 'software' power down with the addition of powering down the Crystal Oscillator to produce 'hardware' power down. The RF Bypass will remain active if it has been previously programmed on the I²C bus. Note that in 'hardware' power down, the I²C interface does not operate.

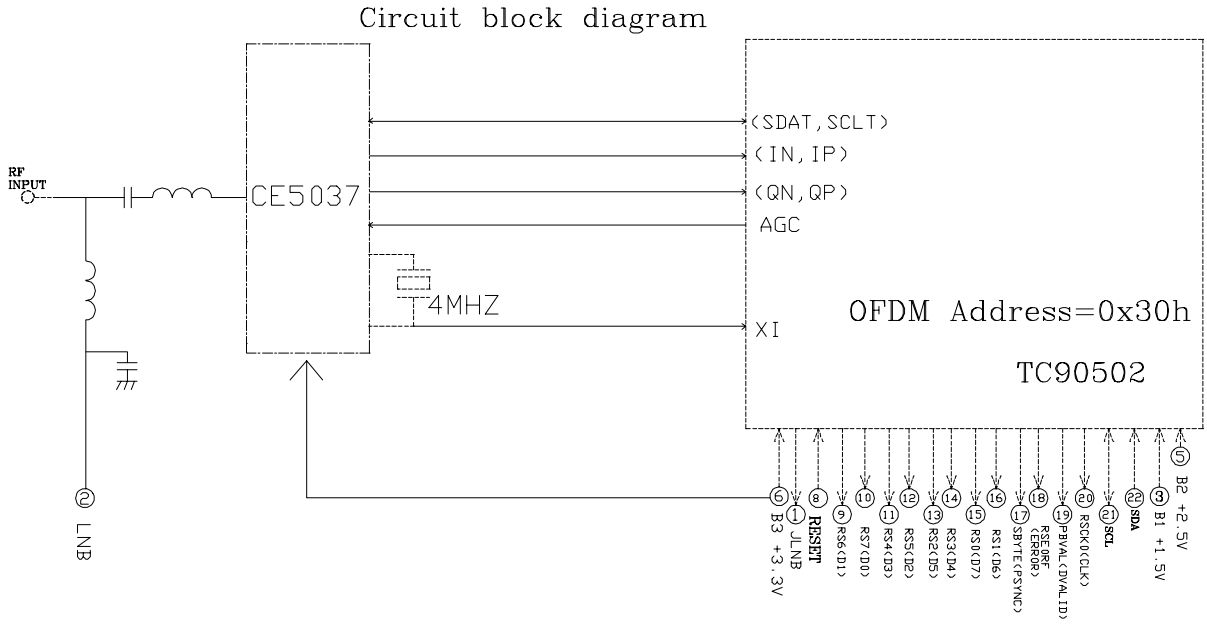
The CLR bit re-triggers the power-on-reset function. This resets all register values to their power-on reset default value. The CLR bit is itself cleared. Note that the chip-wide reset will reset the I²C Interface and the current write sequence used to set this bit will not be acknowledged.

The P0 bit controls the state of the output port according to Table 22.

P0	Output Port State
0	Off, high impedance
1	On, current sinking

Table 22 - Output Port States

Circuit block diagram



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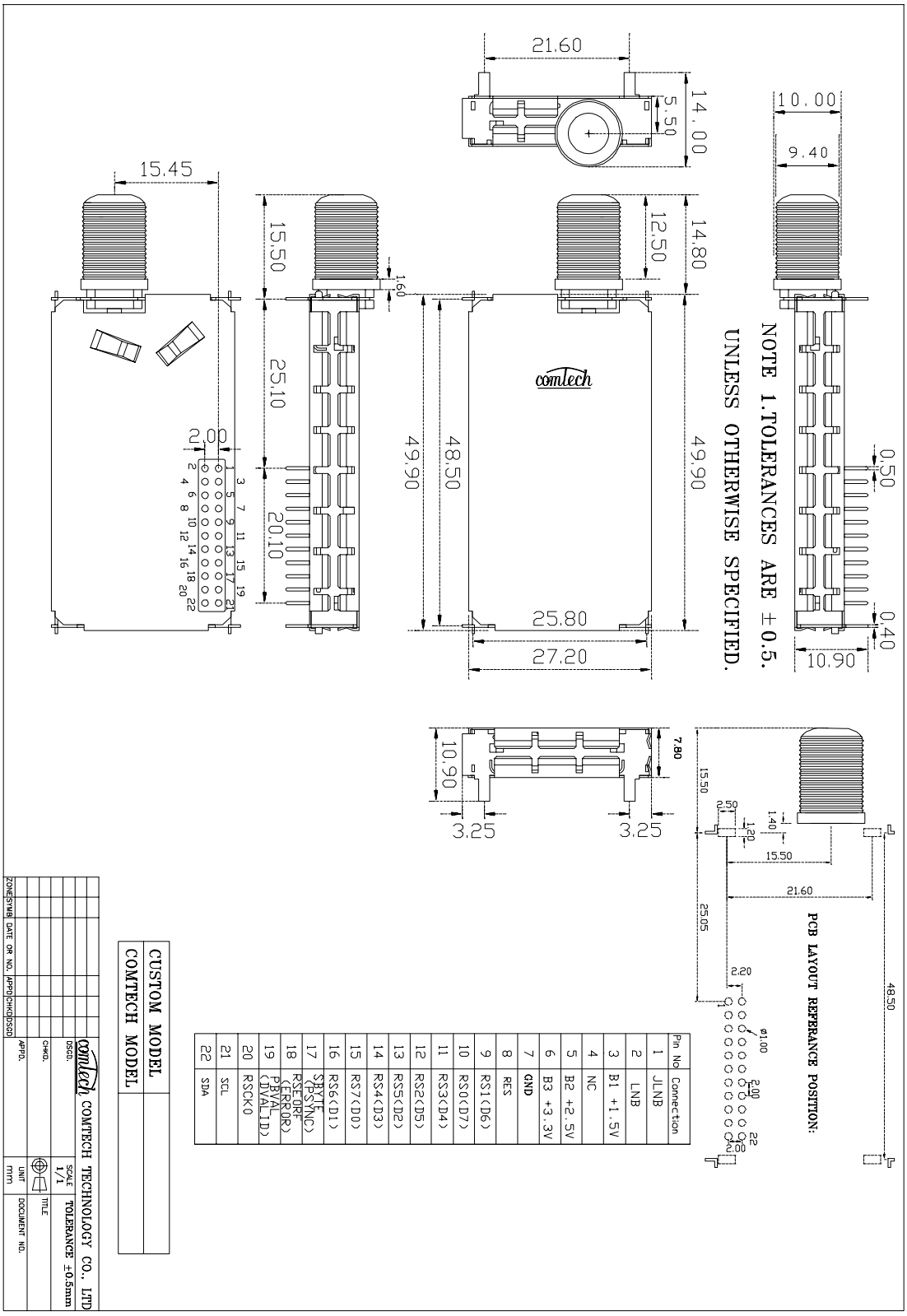

Pin No	Connection
1	JLNB
2	LNB
3	B1 +1.5V
4	NC
5	B2 +2.5V
6	B3 +3.3V
7	GND
8	RES
9	RS1(D6)
10	RS0(D7)
11	RS3(D4)
12	RS2(D5)
13	RS5(D2)
14	RS4(D3)
15	RS7(D0)
16	RS6(D1)
17	SBYTE (PSYNC)
18	RSE ORF (ERROR)
19	PBVAL (DVAL_1D)
20	RSCK0
21	SCL
22	SDA