



SPECIFICATION

DVB-T TUNER

1.SCOPE

The DVBT-782I8ST1FP is intended for the reception of DVB-T compliant MPEG2 signals (full TES 300 744 compliant) in combination with the tuner ,all functions are integrated to deliver a corrected transport stream given DVB-T encoded signal(2k or 8k mode)with 7MHz or 8MHz bandwidth

The DVBT-782I8ST1FP DATA Parallel output from D7 to D0

The tuner can't be used individually, but works together with DVBT-782I8MT1FP because it needs external 20.48MHz clock.

VHF/UHF TUNER,COFDM DEMODULATOR,FOR DVB-T SYSTEM.

LINK IC L64782 has channel filter which can receive B / W : 8MHz or 7MHz OFDM signal.

VHF/UHF TUNER,COFDM DEMODULATOR,FOR DVB-T SYSTEM.

2.GENERAL SPECIFICATIONS

2-1. RECEIVING FREQUENCY RANGE	51~858MHz(I ² C PLL CONTROLLER FROM OUTSIDE)
2-2. SUPPLY VOLTAGE	B+5+/- 0.1V TU 30+/- 1V B+3.3+/-0.08V B+2.5+/- 0.05V
2-3. CONSUMPTION CURRENT	LOOP B+ 5V 50mA TYP B+1 5V 110mA B+2 5V 55 mA B+3 3.3V 50mA B+4 2.5V 400mA
2-4. OPERATION AND STORAGE CONDITIONS FOR GUARANTEE	TEMPERATURE 0~50°C HUMIDITY 85% OR LESS

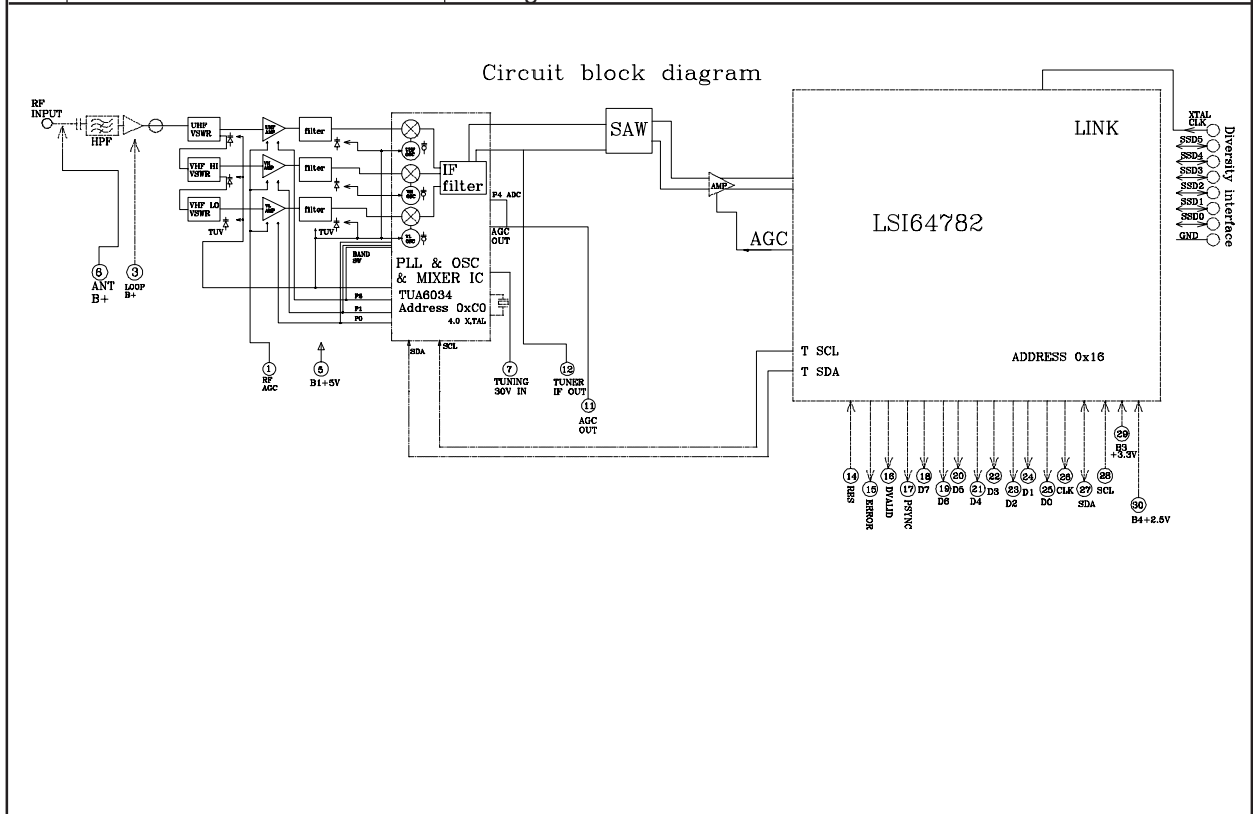
3.TEST CONDITIONS

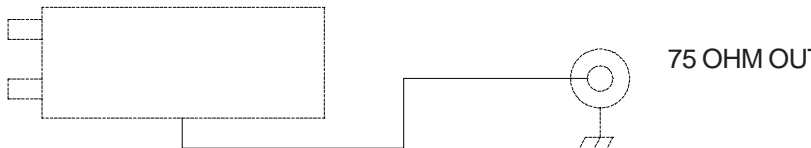
3-1. TESTING AMBIENT CONDITIONS

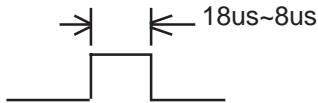
DEFINED AS TEMPERATURE OF 25+/-2°C AND HUMIDITY OF 65+/-5% RH.

NOTE : THAT TEMPERATURES OF 5~30°C AND HUMIDITY OF 45~85% MAY BE REGARDED AS STANDARD.

SPECIFICATION						
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NO	ITEM	CONDITION	MIN	TYP	MAX	NOTES
1.	GENERAL SPECIFICATIONS					
1.1	Receiving frequency range	UHF SEE table 8-12 VHF HIGH SEE table 8-12 VHF LOW SEE table 8-12	428.1 145.1 48		858 428 145	MHz
1.2	Mergin frequency	UHF VHF HIGH VHF LOW	-6 -5 -2		+3 +2 +2	MHz
1.3	RF input Impedance	F CONNECTOR	75 OHM			
1.5	L.O PLL synthesizer IC	TUA6034 Address 0xC0				
1.6	PLL synthesizer crystal	+/- 50 ppm		4.0		MHz
1.7	1st intermediate frequency L64782 AFC_BIAS	DVB-T		36.167		MHz
	3dB BW			0x68=0xDC 0x69=0x3B		
1.10	AGC voltage input external	0V to 5V	0V min gain 5V max gain			Current 20uA max
2	Operating Voltage	Supply voltage	5V +/- 5% 3.3V +/- 5% 2.5 +/- 5%			TUV 28V ~ 33V
2.2	Humidity	Operating	less than 85%			
		Storage	less than 95%			
2.3	Temperature	Operation	0°C to 55°C			
		Storage	-20°C to 75°C%			



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NO.	ITEM	CONDITION	MIN.	TYP.	MAX.	NOTES
TEST CONDITION						
3.	Supply voltage Ambient humidity Ambient temperature	B1 5V, B2, 5V B3 3.3V, B4 2.5V AGC 5V, TUV 28 to 30 V 20°C to 30°C 60% to 70%				
3.1	Test circuit					
3.2	Noise Figure	UHF VHF HIGH VHF LOW		7 6 6	10 9 9	dB dB dB
3.3	AGC Range AGC voltage 5V to 0.5V	UHF VHF HIGH VHF LOW	35 40 45	55 65 65		dB dB dB
3.4	Power gain AGC voltage 5V max gain	UHF VHF HIGH VHF LOW	30 31 32	34 35 38		dB dB dB
3.5	Gain taper				8	dB
3.6	VSWR	UHF VHF HIGH VHF LOW		2 2 2		dB dB dB
3.7	IF Rejection	UHF VHF HIGH VHF LOW	60 60 60	75 80 70		dB dB dB
3.8	Image Rejection	UHF VHF HIGH VHF LOW	50 50 50	55 55 60		dB dB dB
3.9	RF input oscillator leakage	<890 MHz <1800 MHz			34 40	dBuV dBuV
3.10	Phase noise offset 1KHz offset 10KHz offset 100KHz	UHF VHF HIGH VHF LOW UHF VHF HIGH VHF LOW UHF VHF HIGH VHF LOW		-58 -60 -71 -83 -85 -95 -103 -106 -109		dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
3.2	1% cross modulation input Channel +/-2Channel level 60dBuV	UHF VHF HIGH VHF LOW	80 80 80			dBuV dBuV dBuV

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NO	ITEM	CONDITION	NIM	TYP	MAX.	NOTES.
Electrical Characteristics COFDM Demodulator			I ² C Bus intewface to LSI64782 data sheet			
LSI64782 CHIP ADDRESS 16h [00010110]						
5.1	input sensitivity	·Bandwidth 7MHz or 8MHz FET mode 2K Guard interval 1/32 Constllation 64QAm FEC code rate 2/3 RS uncorrected Error=0		-75		dBm
5.2	Performance with AWGN	C/N at antenna input		20		dB
5.3	protection from co-channel PAL	PAL-I 75% color bars,FM sound 1KHz		4		dB
5.4	protection from adjacent channel PAL	PAL-I 75% color bars,FM sound 1KHz		-35		dB
5.5	protection from adjacent DVB-t			-25		dB
5.6	protection from image Channel PAL	PAL-I 75% color bars,FM sound 1KHz		-46		dB
5.7	Performance with single echo inside the interval 2K mode	Te=Tg included (7.2us) Delay phase=0°		1.5		dB
5.8	Performance with single echo inside the interval	Te-Tsymbo 1/2 Delay phase=0°		19.5		dB
5.9	Typical multi-path channel	Additional END		4.0		dB
6.0	<p>Register Control for TSDA and TSCL Pins</p> <p>L64782 Register 39=21 7 set XTR I/O MODE 3A=80</p> <p>Register 34=10 set TSCL=L, TSDA=H 34=20 set TSCL=H, TSDA=L 34=30 set TSCL=H, TSDA=H 34=0 set TSCL=L, TSDA=L</p> <p>It gets better performance by setting up XCTRIO0_0DCTRL as OPEN_DRAIN.</p> <p>To make sure L64782 boot normally, please reset pin LO to HI. and then to LO, HI time at 18us~8us</p> 					

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TABLE 8-4 BIT Read/Write

ADDRESS Btyle	1	1	0	0	0	MA1	MA0	0	A	BYET1
Divider Byte1		14	13	12	11	10	9	8		
	0	2	2	2	2	2	2	2	A	BYTE2
Divider Byte2		7	6	5	4	3	2	1	0	
	2	2	2	2	2	2	2	2	A	BYTE3
Control byte	1	CP	T2	T1	T0	RSA	RSB	OS	A	BYTE4
Bandswitch Byte	0	0	0	P4	P3	P2	P1	P0	A	BYTE5
AGC Control Byte*	ATC	AL2	AL1	AL0	0	0	0	0	A	BYTE6

* Byte6 replaces byte5 when T2,T1,T0=0,1,1

ADDRESS	1	1	0	0	0	MA1	MA0	1	A	BYTE1
STATUS BYTE	POR	FL	1	1	AGC	A2	A1	A0	A	BYTE2

A:ACKNOMLEDGE BIT.

MA1,MA0:VOLTAGE ADDRESS BITS.(Fix MA1,MA0=0,0)

CP:charge pump current bits bit=0 50uA or 125uA

bit=1 250uA(default)or 650uA

see table 8-11 charge pump current

T0,T1,T2:test bits.see table 8-7 test modes

RSA,RSB:reference divider bits see table 8-8 reference divider

OS:tuning control bit bit=0 enable Vt

bit=1 disable Vt

P0,P1,P2,P3:VHFLO,VHFHI,UHF,BANDSWITCH AND ANT SWITCH see table 8-12

P4:NPN port control bit bit=0(fix AGC Voltage input)

ATC:AGC timer constant bit bit=0 time 2S

bit=1 time 50ms

AL0,AL1,AL2:AGC take-over point bits,see table 8-9

POR:power-on reset flag:POR=0 AT POWER-ON

FL:PHASE LOCK DETECT FLAG.bit=1 OSC LOCK

bit=0 OSC UNLOCK

AGC:internal AGC .flag AGC=1 when internal AGC is active (level below 3V)

A0,A1,A2:5-level AGC Voltage

TABLE 8-7 Test modes	T2	T1	T0
Normal mode, charge pump currents 50 and 250uA selectable	0	0	0
Normal mode, charge pump currents 50 and 250uA selectable(default)	0	0	1
CP is in high-impedance state	0	1	0
Byte6 will follow(otherwise byte5 will follow)	0	1	1
P0=Fdiv OUTPUT ,P1=Fref OUTPUT	1	0	0
not in use	1	0	1
Extended mode charge pump currents 50 and 250uA selectable	1	1	0
Extended mode charge pump currents 125 and 650uA selectable	1	1	1

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TABLE 8-8 feferene divider ratios

Reference divider ratios	PLL 4MHz quartz	Mode	T2	T1	RSA	RSB
80	50KHz	normal	0	0	0	0
128	31.25KHz	normal	0	0	0	1
24	166.67KHz	X	X	X	1	0
64	62.5KHz	X	X	X	1	1
32	125KHz	extended	1	1	0	0
28	142.86KHz	extended	1	1	0	1

TABLE 8-9 AGC Take-over point

IF output level symmetrical mode	AL2	AL1	AL0
118 dBuV	0	0	0
115 dBuV	0	0	1
112 dBuV	0	1	0
109 dBuV	0	1	1
106 dBuV	1	0	0
103 dBuV	1	0	1

TABLE 8-10 RF INPUT LEVEL

P4 5-LEVEL ADC (reference)	A2	A1	A0
ANT INPUT LEVEL >110	0	0	0
80~110dBuV	0	0	1
70~80 dBuV	0	1	0
60~70 dBuV	0	1	0
<60 dBuV	1	0	0

TABLE 8-11 charge pump current

Charge pump current	mode	CP	T2	T1	T0
50uA	normal	0	0	0	x
250uA	normal	1	0	0	x
50uA 48~132 MHz 145.1~349 MHz 428.1~659 MHz	extended	0	1	1	0
125uA 132.1~145 MHz 349.1~397 MHz 659.1~759 MHz	extended	0	1	1	1
250uA 397.1~428 MHz 759.1~858 MHz	extended	1	1	1	0
650uA	extended	1	1	1	1

note :x=don't care.

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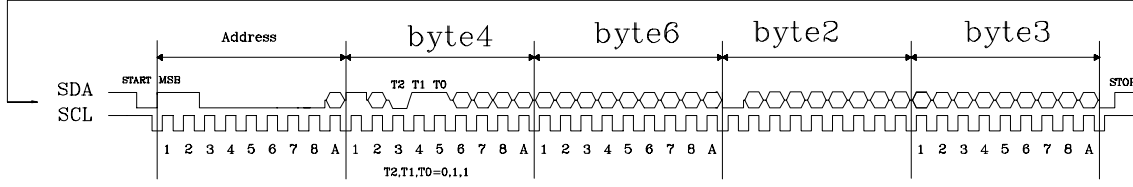
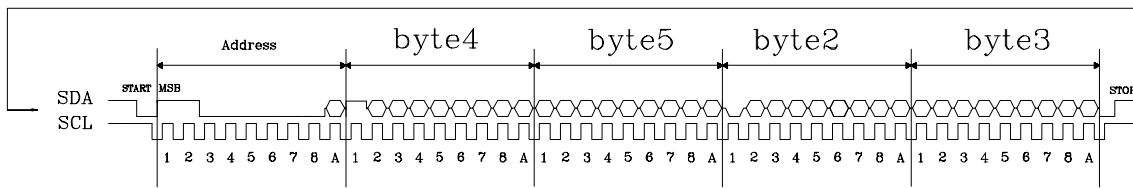
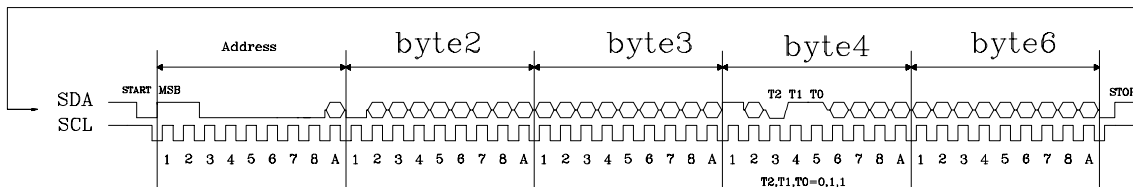
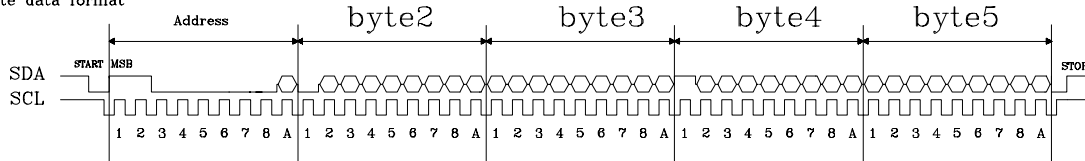
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TABLE 8-12 3-band selection and ANT switch

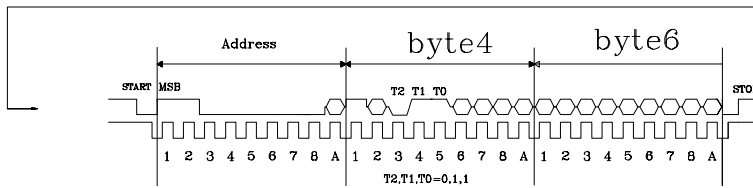
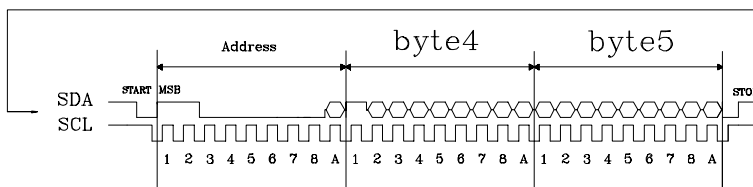
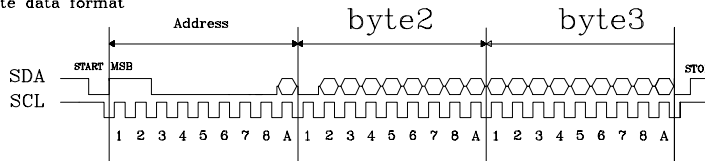
	P0	P1	P3
VHF LO	1	0	0
VHF HI	0	1	0
UHF	0	0	1

I2C BUS Timing Diagram and telegram examples

Write data format



Write data format



SPECIFICATION

DVB-T TUNER

PCB LAYOUT REFERENCE POSITION:

PIN 38,39 GND
PIN 40 20.48MHz CLOCK I/O
Diversity interface I/O
PIN 34,35,36,37
41,42,43

**NOTE 1. TOLERANCES ARE ±0.5.
UNLESS OTHERWISE SPECIFIED.**

PIN NO.	CONTENTS	PIN NO.	CONTENTS
1	AGC IN	17	PSTNG
2	GND	18	D7
3	LOOP B+ 5V	19	D6
4	GND	20	D5
5	B1 5V	21	D4
6	ANT B+	22	D3
7	TUNING 30V IN	23	D2
8		24	D1
9		25	D0
10	B2 5V	26	CLK
11	AGC OUT	27	SDA
12	TUNER IF OUT	28	SCL
13	FEI	29	B3 3.3V
14	RES (H=RES)	30	B4 2.5V
15	ERROR	31	NC
16	DVALID	32	GND

1 AGC IN AGC CONTROL INPUT
3 LB +5V LOOP AMP B+
5 B1 +5V TUNER B+
6 ANT B+ INPUT
7 VT TUNING 30V INPUT
11 AGC CONTROL OUT
12 TUNER 36.167MHz MHZ
13 FEI FRONT-END LOCK
14 RES I64782 RRES†
15 ERROR ERROR SIGNAL
16 DVALID DATA VALID
17 PSTNG PACKET STNG OUT
18-25 D7-D0 DATA OUT
26 CLK BIT CLOCK OUT
27 SDA I2C BUS
28 SCL I2C BUS
29 B3 +3.3V DEMODULATOR B+
30 B4 +2.5V DEMODULATOR B+

CUSTOM MODEL	
COMTECH MODEL	(7/7)

DATE	DR. NO.	APP. / CHECK

SCALE	TITLE
UNIT	DOCUMENT NO.
MM	