SPECIFICATION

DVB-T TUNER

1.SCOPE

The DVBT-782I8MT1FP is intended for the reception of DVB-T compliant MPEG2 signals (full TES 300 744 compliant) in combination with the tuner ,all functions are integrated to deliver a corrected transport stream given DVB-T encoded signal(2k or 8k mode)with 7MHz or 8MHz bandwidth

The DBVT-782I8MT1FP DATA Parallel output from D7 to D0

The tuner can be used separately or co-work with DVBT-782I8ST1FP and set up Diversity for mobile application.

LINK IC L64782 has channel filter which can receive B / W : 8MHz or 7MHz OFDM signal.

VHF/UHF TUNER,COFDM DEMODULATOR,FOR DVB-T SYSTEM.

2.GENERAL SPECIFICATIONS

2-1. RECEIVING FREQUENCY RANGE	51~858MHz(I^2C PLL CONTROLLER FROM OUTSIDE)
2-2. SUPPLY VOLTAGE	B+5+/- 0.1V TU 30+/- 1V B+3.3+/-0.08V B+2.5+/- 0.05V
2-3. CONSUMPTION CURRENT	LOOP B+ 5V 50mA TYP B+1 5V 110mA B+2 5V 55 mA B+3 3.3V 50mA B+4 2.5V 400mA
2-4. OPERATION AND STORAGE CONDITIONS FOR GUARANTEE	TEMPERATURE 0~50^{O}C HUMIDITY 85% OR LESS

3.TEST CONDITIONS

3-1. TESTING AMBIENT CONDITIONS

DEFINED AS TEMPERATURE OF 25+/-2^{O}C AND HUMIDITY OF 65+/-5% RH.

NOTE : THAT TEMPERATURES OF 5~30^{O}C AND HUMIDITY OF 45~85% MAY BE REGARDED AS STANDARD.

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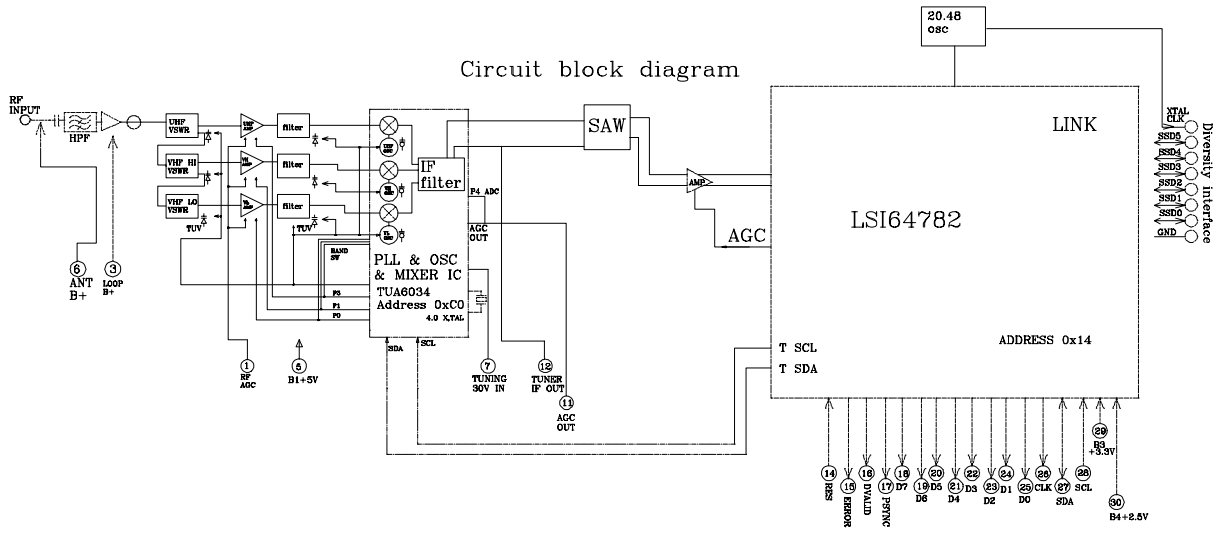
NO	ITEM	CONDITION	MIN	TYP	MAX	NOTES
1.	GENERAL SPECIFICATIONS					
1.1	Receiving frequency range	UHF SEE table 8-12	428.1		858	MHz
		VHF HIGH SEE table 8-12	145.1		428	
		VHF LOW SEE table 8-12	48		145	
1.2	Mergin frequency	UHF	-6		+3	MHz
		VHF HIGH	-5		+2	
		VHF LOW	-2		+2	
1.3	RF input Impedance	F CONNECTOR 75 OHM				
1.5	L.O PLL synthesizer IC	TUA6034 Address 0xC0				
1.6	PLL synthesizer crystal	+/- 50 ppm		4.0		MHz
1.7	1st intermediate frequency	DVB-T		36.167		MHz
	L64782 AFC_BIAS			0x68=0xDC 0x69=0x3B		
	3dB BW			8		MHz
1.10	AGC voltage input external	0V to 5V	0V min gain 5V max gain			Current 20uA max
2	Operating Voltage	Supply voltage	5V +/- 5% 3.3V +/- 5% 2.5 +/- 5% TUV 28V ~ 33V			
2.2	Humidity	Operating	less than 85%			
		Storage	less than 95%			
2.3	Temperature	Operation	0°C to 55°C			
		Storage	-20°C to 75°C%			

Circuit block diagram



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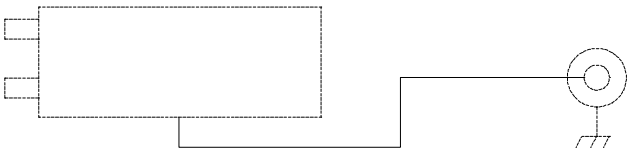
NO.	ITEM	CONDITION	MIN.	TYP.	MAX.	NOTES
	TEST CONDITION					
3.	Supply voltage	B1 5V, B2, 5V B3 3.3V,B4 2.5V				
		AGC 5V,TUV 28 to 30 V				
	Ambient humidity	20°C to 30°C				
	Ambient temperature	60% to 70%				
3.1	Test circuit	 75 OHM OUT				
3.2	Noise Figure	UHF		7	10	dB
		VHF HIGH		6	9	dB
		VHF LOW		6	9	dB
3.3	AGC Range	UHF	35	55		dB
	AGC voltage 5V to 0.5V	VHF HIGH	40	65		dB
		VHF LOW	45	65		dB
3.4	Power gain	UHF	30	34		dB
	AGC voltage 5V max gain	VHF HIGH	31	35		dB
		VHF LOW	32	38		dB
3.5	Gain taper				8	dB
3.6	VSWR	UHF		2		dB
		VHF HIGH		2		dB
		VHF LOW		2		dB
3.7	IF Rejection	UHF	60	75		dB
		VHF HIGH	60	80		dB
		VHF LOW	60	70		dB
3.8	Image Rejection	UHF	50	55		dB
		VHF HIGH	50	55		dB
		VHF LOW	50	60		dB
3.9	RF input oscillator leakage	<890 MHz			34	dBuV
		<1800 MHz			40	dBuV
3.10	Phase noise offset 1KHz	UHF		-58		dBc/Hz
		VHF HIGH		-60		dBc/Hz
		VHF LOW		-71		dBc/Hz
	offset 10KHz	UHF		-83		dBc/Hz
		VHF HIGH		-85		dBc/Hz
		VHF LOW		-95		dBc/Hz
	offset 100KHz	UHF		-103		dBc/Hz
		VHF HIGH		-106		dBc/Hz
		VHF LOW		-109		dBc/Hz
3.2	1% cross modulation	UHF	80			dBuV
	input Channel +/-2Channel	VHF HIGH	80			dBuV
	level 60dBuV	VHF LOW	80			dBuV

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NO	ITEM	CONDITION	NIM	TYP	MAX.	NOTES.
	Electrical Characteristics COFDM Demodulator			I²C Bus intewface to LSI64782 data sheet		
	LSI64782 CHIP ADDRESS 14h [00010100]					
5.1	input sensitivity	·Bandwidth 7MHz or 8MHz FET mode 2K Guard interval 1/32 Constllation 64QAm FEC code rate 2/3 RS uncorrected Error=0		-75		dBm
5.2	Performance with AWGN	C/N at antenna input		20		dB
5.3	protection from co-channel PAL	PAL-I 75% color bars,FM sound 1KHz		4		dB
5.4	protection from adjacent channel PAL	PAL-I 75% color bars,FM sound 1KHz		-35		dB
5.5	protection from adjacent DVB-t			-25		dB
5.6	protection from image Channel PAL	PAL-I 75% color bars,FM sound 1KHz		-46		dB
5.7	Performance with single echo inside the interval 2K mode	Te=Tg included (7.2us) Delay phase=0°		1.5		dB
5.8	Performance with single echo inside the interval	Te-Tsymbo 1/2 Delay phase=0°		19.5		dB
5.9	Typical multi-path channel	Additional END		4.0		dB

6.0 Register Control for TSDA and TSCL Pins

L64782 Register 39=21 set XTR I/0 MODE

3A=80

Register 34=10 set TSCL=L,TSDA=H

34=20 set TSCL=H,TSDA=L

34=30 set TSCL=H,TSDA=H

34=0 set TSCL=L,TSDA=L

It gets better performance by setting up XCTRIO0_0DCTRL as OPEN_DRAIN.

To make sure L64782 boot normally,please reset pin LO to HI.and then to LO, HI time at 18us~8us

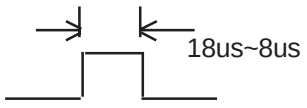

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TABLE 8-4 BIT Read/Write

ADDRESS Btye	1	1	0	0	0	MA1	MA0	0	A	BYET1
Divider Byte1	0	14 2	13 2	12 2	11 2	10 2	9 2	8 2	A	BYTE2
Divider Byte2	7 2	6 2	5 2	4 2	3 2	2 2	1 2	0 2	A	BYTE3
Control byte	1	CP	T2	T1	T0	RSA	RSB	OS	A	BYTE4
Bandswitch Byte	0	0	0	P4	P3	P2	P1	P0	A	BYTE5
AGC Control Byte*	ATC	AL2	AL1	AL0	0	0	0	0	A	BYTE6

* Byte6 replaces byte5 when T2,T1,T0=0,1,1

ADDRESS	1	1	0	0	0	MA1	MA0	1	A	BYTE1
STATUS BYTE	POR	FL	1	1	AGC	A2	A1	A0	A	BYTE2

A:ACKNOMLEDGE BIT.

MA1,MA0:VOLTAGE ADDRESS BITS.(Fix MA1,MA0=0,0)

CP:charge pump current bits bit=0 50uA or 125uA

bit=1 250uA(default)or 650uA

see table 8-11 charge pump current

TO,T1,T2:test bits.see table 8-7 test modes

RSA,RSB:reference divider bits see table 8-8 reference divider

OS:tuning control bit bit=0 enable Vt

bit=1 disable Vt

P0,P1,P2,P3:VHFLO,VHFHI,UHF,BANDSWITCH AND ANT SWITCH see table 8-12

P4:NPN port control bit bit=0(fix AGC Voltage input)

ATC:AGC timer constant bit bit=0 time 2S

bit=1 time 50ms

AL0,AL1,AL2:AGC take-over point bits,see table 8-9

POR:power-on reset flag:POR=0 AT POWER-ON

FL:PHASE LOCK DETECT FLAG.bit=1 OSC LOCK

bit=0 OSC UNLOCK

AGC:internal AGC .flag AGC=1 when internal AGC is active (level below 3V)

A0,A1,A2:5-level AGC Voltage

TABLE 8-7 Test modes	T2	T1	T0
Normal mode, charge pump currents 50 and 250uA selectable	0	0	0
Normal mode, charge pump currents 50 and 250uA selectable(default)	0	0	1
CP is in high-impedance state	0	1	0
Byte6 will follow(otherwise byte5 will follow)	0	1	1
P0=Fdiv OUTPUT ,P1=Fref OUTPUT	1	0	0
not in use	1	0	1
Extended mode charge pump currents 50 and 250uA selectable	1	1	0
Extended mode charge pump currents 125 and 650uA selectable	1	1	1

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TABLE 8-8 feferene divider ratios

Reference divider ratios	PLL 4MHz quartz	Mode	T2	T1	RSA	RSB
80	50KHz	normal	0	0	0	0
128	31.25KHz	normal	0	0	0	1
24	166.67KHz	X	X	X	1	0
64	62.5KHz	X	X	X	1	1
32	125KHz	extended	1	1	0	0
28	142.86KHz	extended	1	1	0	1

TABLE 8-9 AGC Take-over point

IF output level symmetrical mode	AL2	AL1	AL0
118 dBuV	0	0	0
115 dBuV	0	0	1
112 dBuV	0	1	0
109 dBuV	0	1	1
106 dBuV	1	0	0
103 dBuV	1	0	1

TABLE 8-10 RF INPUT LEVEL

P4 5-LEVEL ADC (reference)	A2	A1	A0
ANT INPUT LEVEL >110	0	0	0
80~110dBuV	0	0	1
70~80 dBuV	0	1	0
60~70 dBuV	0	1	0
<60 dBuV	1	0	0

TABLE 8-11 charge pump current

Charge pump current	mode	CP	T2	T1	T0
50uA	normal	0	0	0	x
250uA	normal	1	0	0	x
50uA 48~132 MHz 145.1~349 MHz 428.1~659 MHz	extended	0	1	1	0
125uA 132.1~145 MHz 349.1~397 MHz 659.1~759 MHz	extended	0	1	1	1
250uA 397.1~428 MHz 759.1~858 MHz	extended	1	1	1	0
650uA	extended	1	1	1	1

note :x=don't care.

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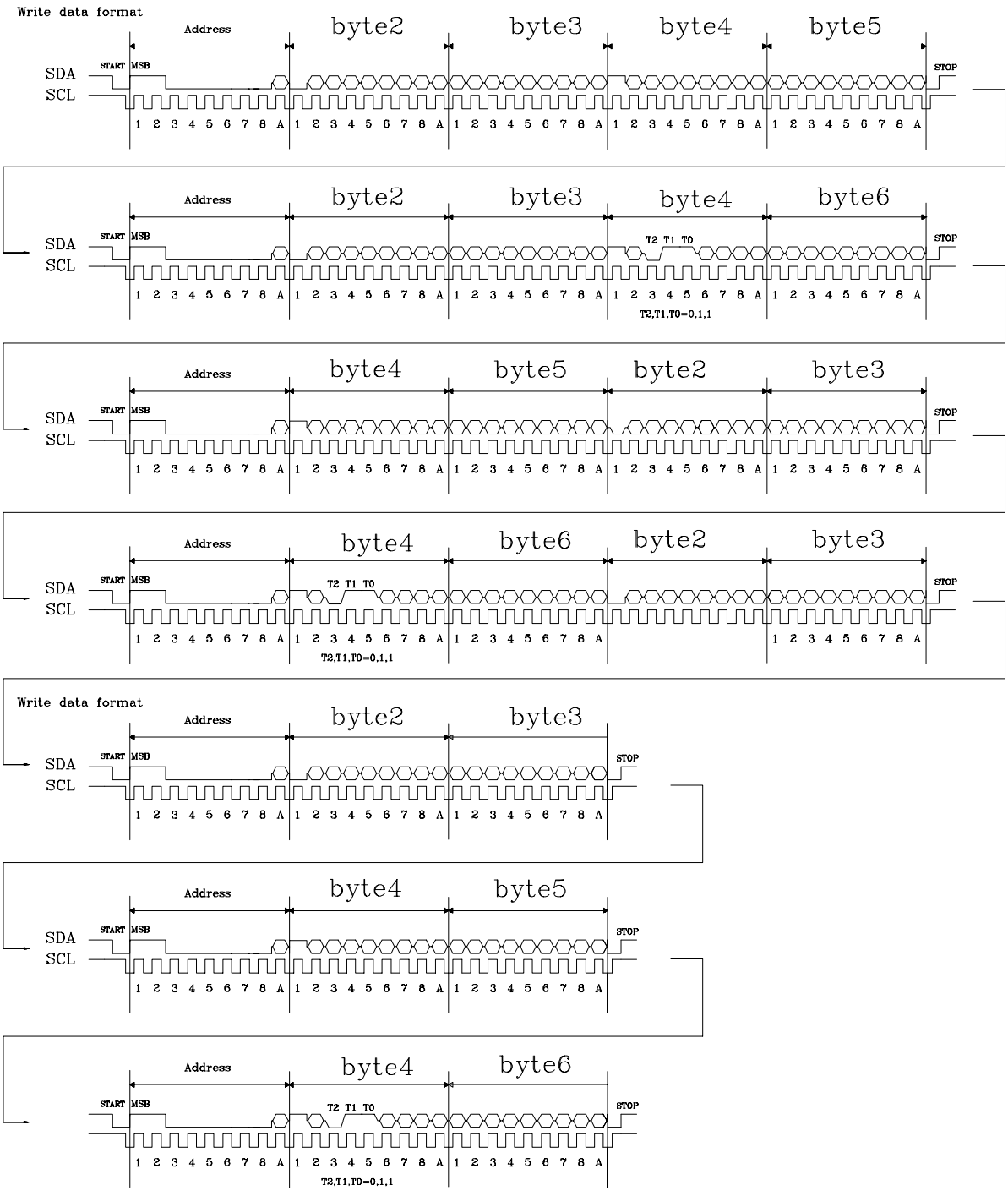
TABLE 8-12 3-band selection and ANT switch

	P0	P1	P3
VHF LO	1	0	0
VHF HI	0	1	0
UHF	0	0	1

I2C BUS Timing Diagram and telegram examples



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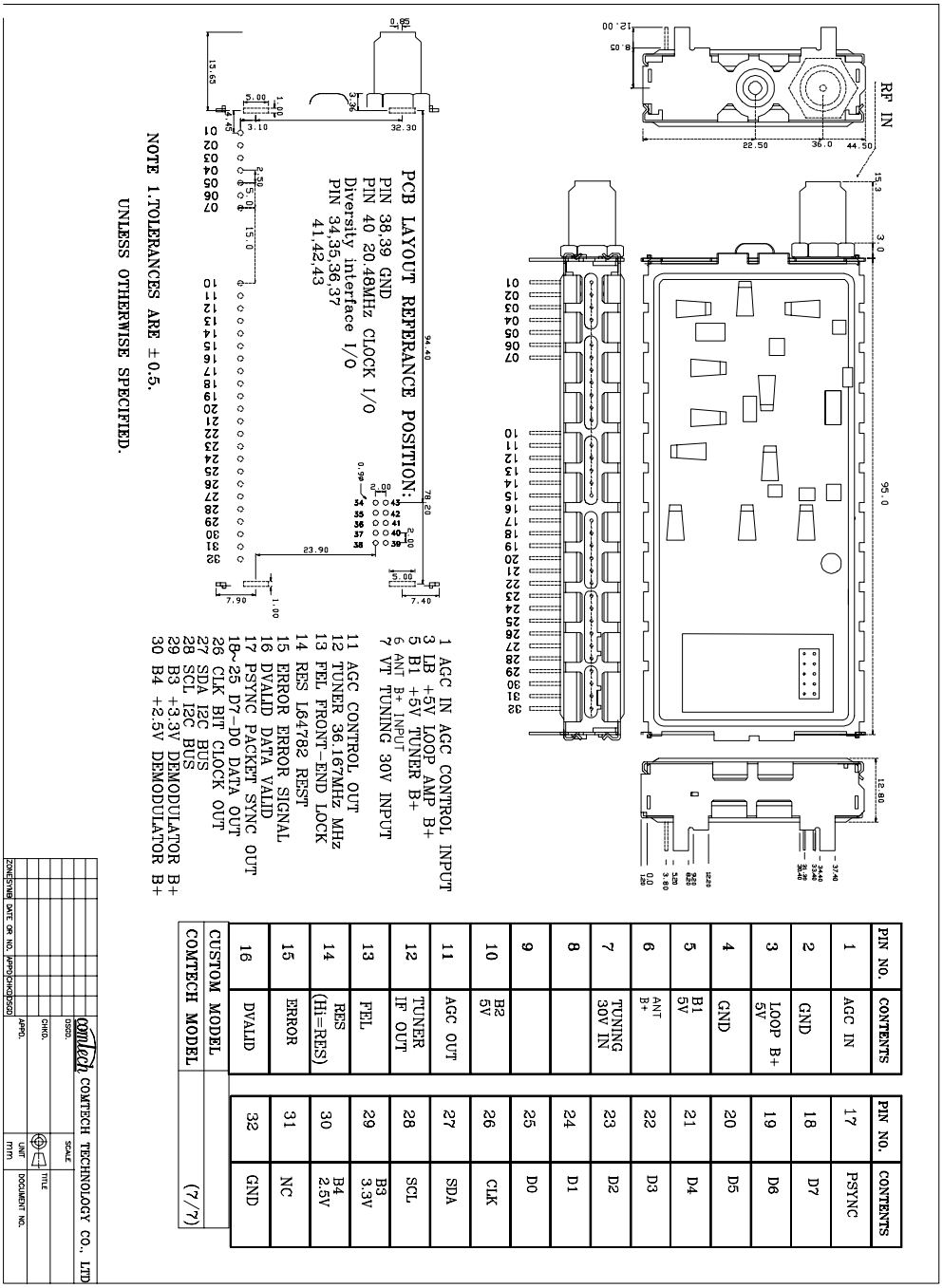

PIN NO.	CONTENTS
1	AGC IN
2	GND
3	LOOP B+ 5V
4	GND
5	B1 5V
6	ANT B+
7	TUNING 30V IN
8	
9	
10	B2 5V
11	AGC OUT
12	TUNER IF OUT
13	FEL
14	RES (Hi=RES)
15	ERROR
16	DVALID

PIN NO.	CONTENTS
17	PSYNC
18	D7
19	D6
20	D5
21	D4
22	D3
23	D2
24	D1
25	D0
26	CLK
27	SDA
28	SCL
29	B3 3.3V
30	B4 2.5V
31	NC
32	GND