



SPECIFICATION																	
BS CONVERTER																	
NO.	ITEM	SPECIFICATION	NOTES														
1-1.	INPUT FREQUENCY RANGE	900.0 MHz-2150.0 MHz	SP5655														
1-2.	ONE INPUT CONNECTOR	F FE-MALE															
1-3.	NOMINAL INPUT IMPEDANCE	75 ohm															
1-4.	TUNING CIRCUIT	BUILT IN PLL															
1-5.	IF FREQUENCY	479.50 MHz CENTER															
1-6.	IF BAND WIDTH	36 MHz															
1-7.	VEDIO OUTPUT POLARITY	POSITIVE GOING															
1-8.	OPERATING VOLTAGE	+28V (+/-5%)(TUNING) +5V (+/-5%)(B+)															
1-9.	OPERATING TEMPERATURE	-10°C ~ +60°C															
1-10.	OPERATING HUMIDITY	LESS THAN 80% R.H.(AT 40°C)															
1-11.	STORAGE TEMPERATURE	-20°C~+70°C															
1-12.	STORAGE HUMIDITY	LESS THAN 95% R.H.(AT 40°C)															
1-13.	INPUT LEVEL	-60~-30dBm															
2.	STANDARD TEST CONDITION	TEST FOR ELECTRICAL SPECIFICATION SHALL BE PREFORMED AT FOLLOWING CONDITION UNLESS OTHERWISE SPECIFIED.															
2-1.	AMBIENT CONDITION	TEMPERATURE 25°C+/-2°C HUMIDITY 65%+/-5%R.H. IF NO DOUBT ON TEST RESULTS, TEMPERATURE +5°C ~ +30°C AND HUMIDITY 45%~80% R.H.COULD BE APPLIED.															
2-2.	MEASUREMENT TO START	30 MINUTES AFTER DC POWER SUPPLIED.															
2-3.	POWER SUPPLY	<table border="1"> <thead> <tr> <th>TERMINAL</th> <th>SUPPLY VOLTAGE</th> </tr> </thead> <tbody> <tr> <td>LNB POWER</td> <td></td> </tr> <tr> <td>+5V</td> <td>+5V(+/-)0.1V</td> </tr> <tr> <td>+28V</td> <td>+28V(+/-)0.1V</td> </tr> <tr> <td>SDA</td> <td>SPECIFIED TUNING</td> </tr> <tr> <td>SCL</td> <td>PULSE.</td> </tr> </tbody> </table>		TERMINAL	SUPPLY VOLTAGE	LNB POWER		+5V	+5V(+/-)0.1V	+28V	+28V(+/-)0.1V	SDA	SPECIFIED TUNING	SCL	PULSE.		
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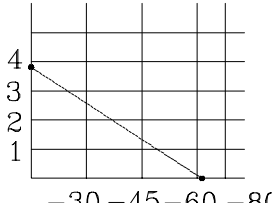


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4.	ABSOLUTE MAXIMUM VOLTAGE	TERMINAL	MAX.SUPPLY VOLTAGE			
		LNB POWER	DC +25V			
		+5V	DC +5.25V			
		+28V	DC +30V			
		SDA,SCL	OV TO THE SAME VOLTAGE AS +5V TERMINAL			
5.	ELECTRICAL SPECIFICATION	TERMINAL	MAX.TAKE OFF CURRENT			
		LNB POWER	500mA			
		UNDER STANDARD TEST CONDITION TEST CHANNEL : DBS 20CH INPUT LEVEL : -45dBm UNLESS OTHERWISE SPECIFICIED.				
		CONDITION	MIN.	TYP.	MAX.	
5-1.	INPUT VSWR	900MHZ-2150MHZ		2.0	3.0	
5-2.	NOISE FIGURE	900.0 MHz				AGC FULLGAIN dB
		~2150MHz		8.0	12.0	
5-3.	LOCAL LEAKAGE AT INPUT TERMINAL	900MHz~-175MHz		-70	-63	dBm
		1750MHz~2150MHz			-50	dBm
5-4.	TUNING VOLTAGE CURVE	900 MHz	1	1.6		V
		950 MHz		2.2		
		1150 MHz		4.0		
		1250 MHz		5.0		
		1450 MHz		7.0		
		1650 MHz		9.2		
		1850 MHz		12.1		
		2050 MHz		15.9		
		2150 MHz		21.0	26.6	
5-5.	LOCAL OSCILLATOR +B SHIFT	TUNING VOLTAGE SHIFT WITH +B +/-5%		+/-10		MHz
5-6.	LOCAL OSCILLATOR TEMPERATURE DRIFH	TUINIG VOLTAGE SHIFT WITH -10°C~+60°C		+/-10		MHz
5-7.	IF 3dB BAND WIDTH			27		MHz
5-8.	Loop through speccification	900MHz~2150MHz				75ohm dB dB dBm dB dB dB dB
5-9.	Output VSWR				2.5	
5-10.	Gain variation		-4		+4	
5-11.	Noise figure			7	10	
5-12.	Spruious st loop through			-70	-63	
5-13.	2nd order intermodulation	at -25dBm input			-35	
5-14.	3rd order intermodulation	at -25dBm input			-50	
5-15.	Isolation RF out to IF test				-20	
5-16.	Isolation RF out to FR in				-20	



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5-17.	Phase noise	10KHz		-75	-70	dB/Hz
		100KHz		-90	-80	dB/Hz
5-18.	POWER GAIN	30				dB



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	(3)SDA,SCL INPUT IMPEDANCE	SDA/SCL ARE IN THE HIGH IMPEDANCE AND THERE SHOULD BE NO RELIABILITY PROBLEM WITH 5V CONTINUALLY ON THE SDA/SCL, IF POWER SUPPLY SUPPLY IS SWITCHED OFF.																																																																																																																						
	(4)DATA FORMAT	<table style="width:100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 25%;"></th> <th colspan="5" style="text-align: center;">MSB</th> <th colspan="5" style="text-align: center;">LSB</th> </tr> </thead> <tbody> <tr> <td>ADDRESS</td> <td>1</td><td>1</td><td>0</td><td>0</td><td>0</td> <td>MA1</td><td>MA0</td><td>0</td><td>A</td><td>BYTE1</td> </tr> <tr> <td>PROGRAMMABLE DIVIDER</td> <td>0</td><td>14</td><td>13</td><td>12</td><td>11</td> <td>10</td><td>9</td><td>8</td><td>A</td><td>BYTE2</td> </tr> <tr> <td>PROGRAMMABLE DIVIDER</td> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td> <td>2</td><td>1</td><td>0</td><td>A</td><td>BYTE3</td> </tr> <tr> <td>CHARGE PUMP AND TEST BITS</td> <td>2</td><td>2</td><td>2</td><td>2</td><td>2</td> <td>2</td><td>2</td><td>2</td><td>(0) OS</td><td>BYTE4</td> </tr> <tr> <td>I/O PORT CONTROL BITS</td> <td>1</td><td>CP</td><td>T1</td><td>T0</td><td>1</td> <td>1</td><td>1</td><td></td><td>A</td><td>BYTE5</td> </tr> <tr> <td></td> <td>P7</td><td>P6</td><td>P5</td><td>P4</td><td>P3</td> <td>P2</td><td>P1</td><td>P0</td><td>A</td><td></td> </tr> </tbody> </table> <p style="text-align: center;">TABLE 1 WRITE DATA FORMAT (MSB IS TRANSMITTED FIRST)</p> <table border="1" style="width:100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 25%;"></th> <th style="width: 10%;">1</th> <th style="width: 10%;">1</th> <th style="width: 10%;">0</th> <th style="width: 10%;">0</th> <th style="width: 10%;">0</th> <th style="width: 10%;">MA1</th> <th style="width: 10%;">MA0</th> <th style="width: 10%;">1</th> <th style="width: 10%;">A</th> <th style="width: 10%;">BYTE1</th> </tr> </thead> <tbody> <tr> <td>ADDRESS</td> <td>1</td><td>1</td><td>0</td><td>0</td><td>0</td> <td>MA1</td><td>MA0</td><td>1</td><td>A</td><td>BYTE1</td> </tr> <tr> <td>STATUS BYTE</td> <td>POR</td><td>FL</td><td>I2</td><td>I1</td><td>I0</td> <td>A2</td><td>A1</td><td>A0</td><td>A</td><td>BYTE2</td> </tr> </tbody> </table> <p style="text-align: center;">TABLE 2 READ DATA FORMAT</p> <p>           A:ACKNOWLEDGE BUT.            MA1,MA0:VOLTAGE ADDRESS BITS.            CP:CHARGE PUMP CURRENT SELECT.            T1:TEST MODE SELECTION.            T0:CHARGE PUMP DISABLE.            OS:VARACTOR DRIVE OUTPUT DISABLE SWITCH.            P7,P6,P5,P4,P3,P2,P1,P0:CONTROL OUTPUT STATES.            POR:POWER ON RESTET INDICATOR            FL:PHASE LOCK DETECT FLAG.            I2,I1,I0:DIGITAL INFORMATION FROM PORTS P7,P5 AND P4.            A2,A1,A0:5 LEVEL ADC DATA FROM P6.         </p>										MSB					LSB					ADDRESS	1	1	0	0	0	MA1	MA0	0	A	BYTE1	PROGRAMMABLE DIVIDER	0	14	13	12	11	10	9	8	A	BYTE2	PROGRAMMABLE DIVIDER	7	6	5	4	3	2	1	0	A	BYTE3	CHARGE PUMP AND TEST BITS	2	2	2	2	2	2	2	2	(0) OS	BYTE4	I/O PORT CONTROL BITS	1	CP	T1	T0	1	1	1		A	BYTE5		P7	P6	P5	P4	P3	P2	P1	P0	A			1	1	0	0	0	MA1	MA0	1	A	BYTE1	ADDRESS	1	1	0	0	0	MA1	MA0	1	A	BYTE1	STATUS BYTE	POR	FL	I2	I1	I0	A2	A1	A0	A	BYTE2
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